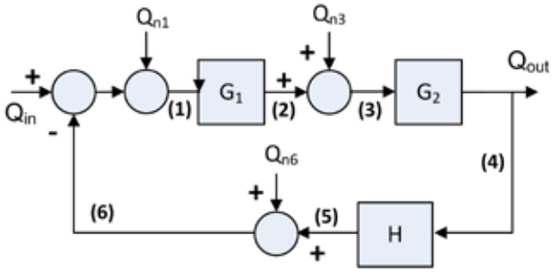
FARRON L. DACUS | RF Design Consultant, Longwing Technology
www.longwingtech.com

Noise and its Shaping in Ultra-Low-Noise Synthesizer Design

This article, the third installment in a five-part series, dives into topics like noise transfer functions and total synthesizer noise.

This is the third article in our low-noise synthesizer design series. Part 1 (Dec. 2018) covered basic design for functionality and stability. Part 2 (Feb. 2019) explored the many noise sources in the synthesizer outside of the actual synthesizer integrated circuit (IC). This third article covers synthesizer IC noise, the closed-loop shaping of noises, and related issues such as optimum bandwidth and synthesizer IC figures of merit. A moderately more complete version will be published online, and still more detail is given in the full version at *www.longwingtech.com*.

This information allows for understanding of how modern synthesizers with on-die voltage-controlled oscillators (VCOs) have been able to displace discrete VCOs for many applications. It also explains when low-noise discrete VCOs offer advantages. Part 4 will review key parts and tools available to the low-noise synthesizer designer. The concluding Part 5 will present low-noise design examples, comparing on-die and discrete VCO results.



1. A generalized feedback tracking loop with noise "Q" injected at various spots is useful for deriving the noise transfer functions from a point "y" to a point "z." Here, the forward gain G is is broken up into G_1 and G_2 for generality.

NOISE TRANSFER FUNCTIONS AND TOTAL SYNTHESIZER NOISE

Part 2 provided the main open-loop noise sources in the phase-locked loop (PLL). Now, we turn our attention to how these noises are shaped by the PLL into the closed-loop noise. We first present a generalized form, using the feedback tracking loop of *Figure 1*.

If we inject noise into any point "y" in the loop, and find the ratio of closed-loop noise on that node to the injected open-loop noise, we will get a generalized version of the highpass "error transfer function," $H_e(s)$, which was given in second-order form in the online version of Part 1:

$$\frac{Q_{nycl}}{Q_{ny}} = H_e(s) = \frac{1}{1+G_1G_2H} = \frac{1}{1+GH} \qquad (1)$$

Another critical function is the "closed-loop transfer function," CL(s), as described by Banerjee:

$$\frac{Q_{out}}{Q_{in}} = CL(s) = \frac{G_1G_2}{1+G_1G_2H} = \frac{G}{1+GH} \qquad (2)$$

This is similar to the classic "phase transfer function" given in older references, differing only as follows:

$$\frac{Q_6}{Q_{in}} = H_{classic}(s) = \frac{G_1G_2H}{1+G_1G_2H} = \frac{GH}{1+GH} \qquad (3)$$

Figures that illustrate $H_e(s)$ and CL(s) are shown in the full version of this article.

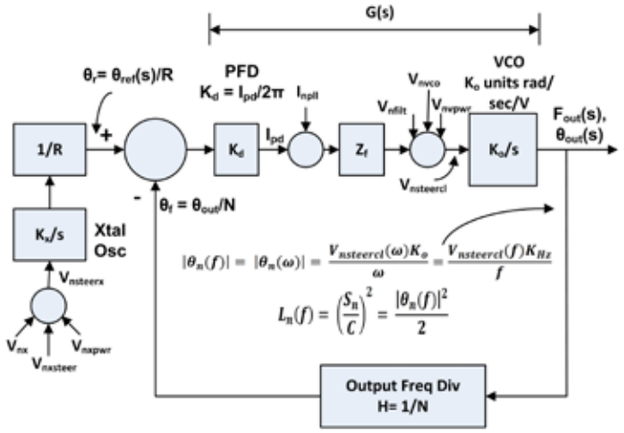
If we examine the noise from any point "y" into which we inject noise Q_{ny} into the loop, to an output node "z," where G_{yz} is the gain from point y to point z, we find:

$$\frac{Q_{nzcl}}{Q_{ny}} = \frac{G_{yz}}{1+G_1G_2H} = \frac{G_{yz}}{1+GH} = G_{yz}H_e(s) \qquad (4)$$

With this generalized information in mind, we may now consider the PLL block diagram of *Figure 2*.

The noise sources of this figure are:

- **V_{nx}:** The steering input referred noise of the crystal reference oscillator itself, from its datasheet, as modified by the VCO noise modulation function to refer this oscillator noise to input.



2. Shown is a general PLL block diagram with noise sources.

- **$V_{nxsteer}$:** The noise of the crystal steering input. Note that standard digital-to-analog converters (DACs) used for this function can be quite noisy.
- **V_{nxpwr}:** The input-referred noise from the crystal-oscillator power supply (see Part 2).
- **K_x:** Steering gain of the crystal reference in rad/sec/V. When referring noise to the xtal oscillator input, K_x should be converted to K_{xHz}.
- **I_{npll}:** The noise of synthesizer chip dividers and charge pump represented as a noise current, derived in the full version.
- **V_{nfilt}:** The output filter voltage noise density presented to the VCO steering input.
- **V_{nvco}:** The Leeson noise of the VCO referred to its steering input.
- **V_{nvpwr}:** The noise effect of VCO power-supply noise referred to the VCO input.

To make use of the transfer-function relationships derived above for the particular PLL case, we will need detailed filter functions. These are given in Table 1 of the full version on the Longwing website. With a particular filter designed and noise sources identified, we have what we need to find the closed-loop noise.

For the PLL block diagram with noise sources as given, we may write for forward gain:

$$G = K_dZ_f\frac{K_o}{s} = \frac{I_{pd}}{2\pi}\frac{K_o}{s}Z_f \qquad (5)$$

The voltage noise or noise sideband to carrier ratio (depending on whether the output node signal is variable in volts or in rad/sec) generated by noise "x" at point "y" is given by:

$$Q_{yz} = G_{yz}H_e = \frac{G_{yz}}{1+GH} = \frac{G_{yz}}{1+\frac{I_{pd}K_o}{2\pi N}Z_f} \qquad (6)$$

We may use this relationship with the input noises to generate the rms sum of closed-loop noises on the VCO input, and then the VCO noise modulation function to give the closed-loop phase noise on the output.

Using the "magnitude" function to emphasize these are rms noise quantities, the reference noise at the VCO input will be:

$$|V_{nxcl}| = \left|\frac{K_x}{s}\frac{1}{R}Z_f\,H_e\right| \qquad (7)$$

The noise from the charge pump and dividers of the synthesizer chip is normally handled directly at the VCO output using methods developed by Banerjee. These methods shall be presented later, but first we will develop the method of summing all noise sources to get total phase noise.

We assume here that we have a frequency-dependent current-noise function, i_{npll}, that can be summed into the loop filter. This noise-current function is derived from the Banerjee model in the full-length version. The noise voltage at the VCO input from the charge pump and divider noise is:

$$|V_{npllcl}| = |I_{npll}Z_fH_e| \qquad (8)$$

The closed-loop noises for the loop filter, input-referred VCO noise, and input-referred VCO power-supply noise are all on the VCO input, and are therefore simply the open-loop noises multiplied by H_e:

$$|V_{nfiltcl}| = |V_{nfilt}H_e(s)| \qquad (9)$$

$$|V_{nvcocl}| = |V_{nvco}H_e(s)| \qquad (10)$$

$$|V_{nvpwrcl}| = |V_{nvpwr}H_e(s)| \qquad (11)$$

Separately graphing each of these quantities over frequency is highly enlightening as to which terms are dominant, or worth more design effort and parts cost to reduce.

The magnitude of the total noise on the VCO steering input is given by the rms sum of the above sources:

$$|V_{nsteer}| = \sqrt{|V_{nxcl}|^2 + |V_{npllcl}|^2 + |V_{nfiltcl}|^2 + |V_{nvcocl}|^2 + |V_{nvpwrcl}|^2} \qquad (12)$$

Finally, this rms summed total noise voltage on the VCO input in the closed-loop state is transformed to a total output phase noise using the VCO modulation function.

CHARGE PUMP AND DIVIDER NOISE AND CORNER, SYNTHESIZER IC FIGURE OF MERIT, AND MODELING

This synthesizer IC charge pump and divider noise is often called "PLL noise," a term avoided here because confusion could arise as to whether this is total PLL noise. Instead, we use the term "CPD noise."

Flat Synthesizer Noise

First subjected to systematic deep analysis by Banerjee (Ref. 3), the physical source of this noise is the charge pumps and dividers, shaped by closed-loop action to often appear relatively flat over frequency. In recent years, this noise has dropped significantly.

We can intuitively understand this noise as follows. For any given pulse width with a given jitter, we can hypothesize that there will be a floor to this noise, a term proportional to the comparison frequency (number of the narrow pulses per unit of time), and a multiplication term similar to that of multiplying the crystal-reference phase noise. The resulting "flat" noise (neglecting 1/f at low-frequency offsets) is given by:

$$L_{flatdB}(f) = PN1HzdB + 20log|CL(f)| + 10log(f_{comp}) \quad (13)$$

Here, "PN1Hz" is the normalized floor on a per Hz basis. It's typically given in dB, but we will have occasion to convert it to linear. The empirical approach that supports this equation is proven in Ref. 4, in which a timing jitter analysis leads to the same results. Inside the loop bandwidth, **CL(f) ~ N**, and:

$$L_{flatdB}(f) = PN1HzdB + 20logN + 10log(f_{comp}) \quad (14)$$

Because $N = f_{out}/f_{comp}$, we may write:

$$L_{flatdB}(f) = PN1HzdB + 20log(f_{out}) - 10log(f_{comp}) \quad (15)$$

Since there's noise in each phase detector pulse, the 3-dB reduction of in-band noise for each doubling of f_{comp} in the above relation may seem odd. Doubling f_{comp} adds 3 dB to the noise contributed by the phase detector pulses. However, doubling f_{comp} also reduces N by two, which removes 6 dB of noise multiplication. The net is the 3-dB improvement shown.

This simple equation has powerful results for the synthesizer industry. We are normally given f_{out}, and by using a smaller N value, we get higher f_{comp} and lower in-band phase noise while generating that f_{out}. This is the method being strongly applied by semiconductor companies with modern sigma-delta fractional N synthesizers, with comparison frequencies now up to 100 to 200 MHz (Part 4) and high loop bandwidths. The high in-band noise suppression achieved is key to allowing higher-noise on-die VCOs to have effectively low noise at required phase noise offsets.

Flicker Synthesizer Noise

The method often used to model 1/f noise in the synthesizer chip is to assume that in-band noise at 10 kHz is dominated by flicker, and to scale that noise by output frequency relative to 1 GHz and by offset relative to 10 kHz. This gives:

$$L_{flickerdB}(f) = PN_{1-fdB} + 20log\left(\frac{f_{out}}{1E9}\right) - 10log\left(\frac{f_{off}}{1E4}\right) = PN_{1_{fdB}} + 20log(f_{out}) - 10log(f_{off}) - 140dB \quad (16)$$

The term PN_{1_f} is used by Analog Devices *(www.analog.com)* as a 1/f noise parameter. Texas Instruments *(www.ti.com)* refers to this same term as $PN_{PLL\_1/f}$. Linear Technology (acquired by Analog Devices) instead eliminates the referencing to 1-GHz carrier and 10-kHZ offset. They use the normalized 1/f noise term $L_{M(NORM-1/f)}$. Let's refer to this term with the simpler variables $PN_{flicker}$ and $PN_{flickerdB}$. Their equation is:

$$L_{flickerdB}(f) = PN_{flickerdB} + 20log(f_{out}) - 10log(f_{off}) \quad (17)$$

Comparing these two equations, it's seen that:

$$PN_{flickerdB} = PN_{1\_fdB} - 140dB \quad (18)$$

$$PN_{flicker} = \frac{PN_{1\_f}}{1E14} \quad (19)$$

Combining Flat and 1/f Synthesizer Noise

To add flat power to flicker power to get a total synthesizer chip noise power, we need linear terms, which are:

$$L_{flat} = PN_{flat} = PN1Hz\,|CL(f)|^2 f_{comp} \quad (20)$$

Within the loop bandwidth:

$$L_{flat} = PN_{flat} = PN1Hz\,N^2 f_{comp} \quad (21)$$

$$L_{flicker} = PN_{flicker}\frac{f_{out}^2}{f_{off}} = \frac{PN_{1-f}\,f_{out}^2}{1E14\;f_{off}} \quad (22)$$

The total charge pump and divider noise at $f = f_{off}$ is given by:

$$L_{cpdtot} = L_{flat} + L_{flicker} \quad (23)$$

Assuming that the flicker corner is within the loop bandwidth, we may set the flicker and flat noises equal to solve for corner frequency at a particular output frequency, N, and f_{comp}. When we do this and substitute $N = f_{out}/f_{comp}$, we get as the closed-loop noise corner due to synthesizer IC 1/f noise:

$$f_{npllcorner} = \frac{PN_{flicker} f_{comp}}{PN1Hz} = \frac{PN_{1-f}}{1E14}\,\frac{f_{comp}}{PN1Hz} \quad (24)$$

Current Noise Model

The above noises are expressed on the VCO output in the closed-loop state. Synthesizer CPD noise can be expressed as a sum of a flat and 1/f noise current injected into the loop filter in parallel with a then assumed noise-free charge-pump current. This form is useful for SPICE modeling of the synthesizer noise. The analysis to determine this noise is given in the full version. The results for the combined flat and 1/f noise are:

$$i_{npltot} = \frac{\sqrt{2}\,I_{pd}}{2\pi}\sqrt{PN1Hz\,f_{comp}}\sqrt{1 + \frac{f_{npllcorner}}{f}} \quad (25)$$

Synthesizer IC Noise Figure of Merit

If the synthesizer chip noise current, i_{npltot}, is integrated from 1 Hz to f_L, we obtain a synthesizer IC noise power figure of merit:

$$IC_{nfom} = \frac{I_{pd}^2}{2\pi^2} f_{comp}\left(PN1Hz\,f_L + f_{comp}\,PN_{flicker}\,ln(f_L)\right) \quad (26)$$

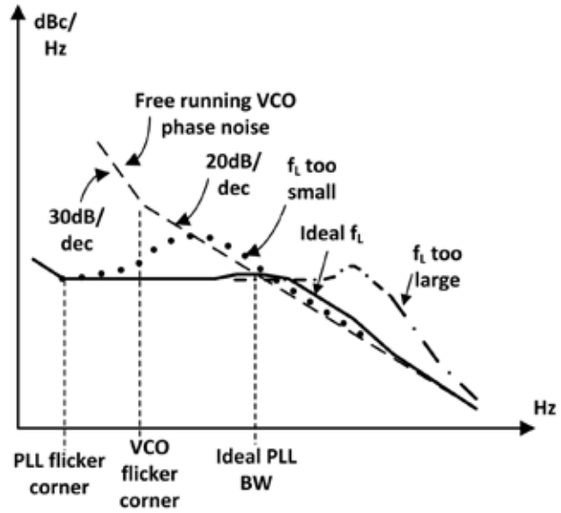
Any time we are comparing two ICs with the same I_{pd} and f_{comp}, the figure of merit may be simplified to:

$$IC_{nfom} = PN1Hz\,f_L + f_{comp}\,PN_{flicker}\,ln(f_L) \quad (27)$$

These figures of merit allow for comparing the total integrated in-band noise due to the synthesizer IC, taking into account variations in floor and corner that could disguise which IC may have the lowest total noise for a particular application.

OPTIMUM LOOP BANDWIDTH COUNTING ALL NOISE SOURCES

The "ideal bandwidth" generally means a bandwidth in which the typically nearly flat in-band noise intersects the VCO free-running noise at the loop bandwidth. A lower bandwidth would mean that the VCO noise at the loop bandwidth is higher than the flat in-band noise. It will look like significant noise peaking around the loop bandwidth as that noise is suppressed moving down into the loop bandwidth. A higher bandwidth will mean that the noise induced by the synthesizer IC will be higher than the VCO free-running noise at the loop bandwidth. These effects are shown in *Figure 3*.



3. This is an illustration of ideal bandwidth versus noise effects of too small or large a bandwidth.

Ideal Passive BW for VCO Noise and Flat Synthesizer IC Noise Only

Ignoring any noise modulation of the VCO by the loop filter and the flicker corner of the synthesizer IC, we can easily find the approximate ideal bandwidth from setting $L_{flat} = L_{VCO}$ and solving for f. This is the approximate approach recommended by Banerjee (Ref. 3, 5th edition, pp. 305-306).

Assuming the desired f_L will be on the –20 dB/dec part of the phase noise slope, and that we know the phase noise $L(f_{ref})$, the VCO noise at a frequency f_L (the desired bandwidth) will be given by:

$$P_{nvco} = L(f_{ref})\frac{f_{ref}^2}{f_L^2} = PN_{flat} \quad (28)$$

The ideal bandwidth $f_{L\text{-}VCO}$, considering only VCO noise, then is:

$$f_{L-VCO} = f_{ref}\sqrt{\frac{L(f_{ref})}{PN_{flat}}} \quad (29)$$

Ideal BW with the Passive Loop Filter Including Synthesizer and VCO Flicker Noises

We get a more accurate measure of the optimum minimum jitter bandwidth when these noise sources are considered. These noise sources may lead to either an *increase or decrease* in ideal bandwidth to that predicted using VCO noise alone. Adding loop-filter noises and VCO flicker noises will push out the ideal bandwidth. But, counting in the higher synthesizer IC noise with synthesizer flicker tends to push toward a lower intersection.

When we consider ideal bandwidth with the noise of a filter added to the VCO noise, in the frequency range where

the bandwidth f_L will fall on the −20 dB/dec part of the VCO phase noise, and take into account synthesizer flicker noise, we may write:

$$P_{nvco} + P_{nfilt} = L_{flat} + L_{flicker} =$$

$$PN1Hz\, N^2 f_{comp} + PN_{flicker} \frac{f_{out}^2}{f_L} \qquad (30)$$

For the passive filter, the noise comes from the resistors in the filter. We are mostly interested in the noise at the loop bandwidth, where it's neither suppressed by the loop or filtered off by higher-order poles. At this frequency, using the thermal noise and the VCO noise-modulation function:

$$P_{nfilt} = \frac{M4kTR_2 K_{Hz}^2}{2f_L^2} \qquad (31)$$

In this equation for P_{nfilt}, "M" is a multiplier for filter form. M = 1 for the first- and second-order filter (only R_2), M is generally about 2 to 3 for the third-order form (adding R_3), and generally about 3 to 4 for the fourth-order form (adding R3 and R4). Now, we can get a good approximation for R_2 from the second-order PLL equations, where:

$$R_2 \cong \frac{2\pi N f_L}{K_{Hz} I_{pd}} \qquad (32)$$

Substituting this into the equation for passive filter noise:

$$P_{nfilt} = \frac{M4\pi kTNK_{Hz}}{f_L I_{pd}} \qquad (33)$$

We may substitute this relation for P_{nfilt} and the linear expressions for P_{nvco} and P_{nflat} into Equation 31, and solve for ideal bandwidth f_L. Because the expression for P_{nvco} as a function of frequency is second order, the expression for P_{nfilt} is first order, and the expression for Pnflat is constant, we end up with a quadratic equation:

$$P_{nflat} f_L^2 - \left(\frac{M4\pi kTNK_{Hz}}{I_{pd}} - P_{nflicker} f_{out}^2\right) f_L -$$

$$L_{vco}(f_{ref}) f_{ref}^2 = 0 \qquad (34)$$

Since this solution to this quadratic will always have a positive and negative frequency result, there's never any doubt as to the correct root.

Note in the above that it was assumed that the final bandwidth was at a frequency greater than the VCO flicker corner. This is often—but not always—true. If the final bandwidth calculated using the above is in fact below the VCO flicker corner, then we must modify our design procedure. This is shown in the full-length version, and results in a cubic relation for the bandwidth.

Ideal Bandwidth for the Slow Slew Active Loop Filter

This inverting form loop filter is the most recommended for higher-voltage-tune-range VCOs. An expression for the noise terms in the output of this filter was derived in the full-length version of Part 2 (Ref. 2). For the reasons given in the full-length version of this article, we may ignore the noise contributions of R_3 and R_4 when finding ideal bandwidth. Thus, the filter noises we use are:

$$V_{noptot}^2 = G_{n1}^2 V_{np}^2 + V_{nopR2}^2 + V_{nopInop}^2 \qquad (35)$$

Next, we translate this noise to VCO output using the VCO noise-modulation function, which gives:

$$P_{nfilt} = \frac{G_{n1}^2 V_{np}^2 K_{Hz}^2}{2f_L^2} + \frac{4\pi kTNK_{Hz}}{I_{pd} f_L} + \frac{i_{nop}^2 2\pi^2 N^2}{I_{pd}^2} \qquad (36)$$

We recall the VCO noise, including noise below its flicker corner as:

$$P_{nvco} = L(f_{cvco}) \frac{f_{cvco}^3}{f_L^3} + L(f_{ref}) \frac{f_{ref}^2}{f_L^2} \qquad (37)$$

The main equation to be used to set VCO and filter noise equal to synthesizer IC noise at the loop bandwidth f_L is:

$$P_{nvco} + P_{nfilt} = L_{flat} + L_{flicker} =$$

$$PN1Hz\, N^2 f_{comp} + PN_{flicker} \frac{f_{out}^2}{f_L} \qquad (38)$$

The above equations may be combined to give this equation cubic in f_L:

$$\left(\frac{2\pi^2 i_{nop}^2 N^2}{I_{pd}^2} - P_{nflat}\right) f_L^3 + \left(\frac{4\pi kTNK_{Hz}}{I_{pd}} - P_{nflicker} f_{out}^2\right) f_L^2 + \left(\frac{G_{n1}^2 V_{np}^2}{2}\right.$$

$$\left. L_{vco}(f_{ref}) f_{ref}^2\right) f_L + L_{vco}(f_{cvco}) f_{cvco}^3 = 0$$

(39)

Here, the noise gain G_{n1} from op amp plus input to op-amp output at the loop bandwidth is given by:

$$G_{n1}^2 = \frac{V_{nopp}^2}{V_{np}^2} = \left|1 + \frac{Z_{for}}{Z_{back}}\right|^2 \cong 1 \qquad (40)$$

The expressions for Z_{for} and Z_{back} developed in the full-length version of Part 2 may be approximated at f_L as below:

$$Z_{back} = R_3 + \frac{1}{sC_3R_3} = \frac{sC_3R_3+1}{sC_3} \cong \frac{1}{j2\pi f_L C_3} \; (at\, f_L) \qquad (41)$$

$$Z_{for} = \frac{1+sR_2C_2}{s(C_1+C_2+sR_2C_2C_1)} \cong R_2 \; (at\, f_L) \qquad (42)$$

The above cubic relationship for f_L is to the author's knowledge the most accurate published relationship for getting an initial value for ideal loop bandwidth, as it takes all of the major factors into account. However, it still relies on several approximations, which are discussed in the full-length version along with more detailed analysis recommendations and a simplified version of this equation.

Ideal Bandwidth for the Semi-Active Buffered Loop Filter

The ideal bandwidth for this filter form is analyzed in the full version.

SPICE MODELING OF SYNTHESIZERS AND THEIR NOISE

The mathematical analysis is more flexible than SPICE, but it's quite a chore to juggle all of the noise sources and control system behaviors described above. A combination system (block) and circuit-level SPICE analysis can confirm the correctness of the mathematical analysis and can often be more accurate. Methods for using SPICE for PLL noise analysis are given in the full version.

SPUR NOISE

Spurs are discrete frequency components most commonly caused by digital noise on the phase detector output that get through the loop filter in at least noticeable form and cause modulation on the input of the VCO. These are discussed in the full version, and in greater detail in the references given there.

SYSTEM PHASE NOISE REQUIREMENTS

Approximate requirements for some applications are derived in the full-length version.

SUMMARY

This article has shown how the noise of the VCO can be significantly suppressed inside the loop bandwidth. Selecting the ideal loop bandwidth for the loop-filter type in use, and the synthesizer with the best figure of merit, will result in the lowest total integrated noise. Noise suppression with high-speed sigma-delta synthesizers allow even the noise of on-die VCOs to be suppressed to the point of now allowing fully integrated synthesizers for most applications (to be demonstrated in Part 5).

The long version of this article at *www.longwingtech.com* shows methods of synthesizer-noise specification that can show when an active loop filter and discrete VCO solution is necessary. MW

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