

# Key Parts for Ultra-Low Noise Synthesizer Design

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## Introduction

This is the 4th part in our low noise synthesizer design series. This is the long version with extra information posted at [www.longwingtech.com](http://www.longwingtech.com). A shorter print and digital version was published at "Microwaves & RF".

Article 1 introduced advanced loop design for desired loop bandwidth and phase margin in the presence of higher order filters, and included both passive and active filters. Article 2 covered noise sources in the loop outside of the synthesizer IC. Article 3 added synthesizer IC noises and how they are modeled, and how all the noise sources for both passive and active loop filters are combined and shaped by the loop. This article will cover the key parts and tools needed by design engineers seeking the lowest noise designs, which include some recently introduced parts and subsystems allowing better performance than the recent past. It was the modern delta-sigma synthesizer IC that served as the foundation of the recent major advances in synthesizer technology, and it drove the development of essential supporting parts. Naturally the designer is concerned with the cost trade-offs of these key parts, so that is presented in some detail here, from the point of view of surveying what the market now offers rather than describing design methods in high detail. Part 5 will bring it all together in the form of low noise examples, comparing and contrasting the performance attained by the various methods and available parts.

## Key Components

**Major Trends:** The top trend driving lower noise in modern single loop synthesizers is the development of the delta-sigma synthesizer IC in very high-speed IC processes. This synthesizer approach allows fractional N synthesis, featuring real number multiplication and not just integer multiplication of the reference frequency, with high resolution frequency stepping and low spurs. With large and highly competitive markets at stake, some of the exact design methodologies of these synthesizer IC's are generally maintained as proprietary. However, an excellent review of many of these methodologies as of 2016 is given in Ref. 5.

The key breakthrough is that high fractional resolution allows high frequency references, which in turn allows high bandwidth for maximum noise suppression inside a much wider loop bandwidth than integer synthesizers allow for. Since the value of the key  $R_2$  (see earlier articles) loop filter resistor is proportional to bandwidth, high bandwidth tends to push  $R_2$  and its thermal noise impact on phase noise higher, but since  $R_2$  is also proportional to N, the low N value of the delta-sigma synthesizer counteracts this.

The ability to use higher reference frequency has driven those references to become available—a situation of positively reinforcing cause and effect that stack up to doubly benefit the design of

low noise synthesizers. Integer N synthesizer crystal references were usually in the range of 1MHz to 20MHz (10MHz being a popular choice), with divided frequency steps usually in the range of 1kHz to 200kHz as per system requirements. But, the ability of the fractional N synthesizer to effectively hit any frequency with only small error (less than the ppm accuracy of the crystal) allows the use of higher frequency references, leading to increasing market demand for these references. Crystal oscillators as high as 100MHz are now becoming available at cost effective prices, and many synthesizers allow internal doubling to 200MHz to allow still higher loop bandwidths. With reduced pricing for 100MHz oven-controlled references made in higher volume, and the recent arrival of cost effective 100MHz voltage controlled temperature compensated crystal oscillators (VCTCXO's) featuring very low phase noise, the cost to get the benefits of the higher loop bandwidths has become reasonable for many applications.

The ability to suppress noise with wider loop bandwidth also rendered on-die VCO's as practical, and spurred their development, notably featuring multiple on-die VCO's each with high numbers of switched resonators that in combination allow a high tune range. That 2-16GHz example of Ref. 5 includes four separate VCO cores, each with 32 different resonator settings that are attained by switching the resonator capacitors of each VCO. This keeps the tune slope moderate to contain induced noise, and switching whole VCO's as well allows maintaining a near optimum L to C ratio for minimum phase noise. The small tune range needed for each resonator setting also allows for tune voltage to be limited to the high end of the power supply range to keep large RF swing (also needed for lower phase noise) from forward biasing tuning varactors. Using switched resonator parts is generally impractical for high Q resonators on discrete VCO's since the transistor switch impedance will strongly degrade the high Q, but with the modest Q of on-die resonators the degradation is also modest. Though the resulting Q of the on-die resonators is lower and thus noisier than the discrete VCO can provide, this approach still provides the lower induced noise (via baseband noise on the tune port) levels of narrowband VCO's while externally looking like a wideband VCO.

The resulting on-die noise performance above about 4GHz can generally match or beat the best octave bandwidth discrete VCO's. The best octave bandwidth VCO's below 4GHz can currently outperform on-die narrowband emulations of wideband VCO's by about 2 to 8dB, while the best narrowband VCO's can exceed on-die performance by 10 to 30dB. These can be strong advantages for phase noise around and past the loop bandwidth. However, the current market situation of the very lowest PLL noise (charge pump and divider noise) being available only with on-die VCO's limits the ability of discrete VCO's to provide better noise within the loop bandwidth than that of the very best on-die VCO synthesizers. As of late 2019 the difference in PLL noise between the best on-die VCO synthesizers and the best external VCO synthesizers is approximately 3-4 dB. The discrete VCO approach also faces cost challenges in that many of the best discrete VCO's require higher supply and tune voltages that take extra components. Low noise regulator and op amp parts are available for this purpose, but they are adding to bill of material cost and board area. Still, when phase noise around and past the loop bandwidth must be the best possible, then the discrete VCO remains the choice.

## **Synthesizer IC's**

Among the key issues for choosing among modern delta-sigma synthesizers are their internal noise parameters, which model the noise that the charge pump and dividers induce on the VCO in the closed loop state. These are described in detail in Part 3 of this series (Ref. 3), but are

modeled as a flat and 1/f noise term for each part. “PN1Hz” is the normalized floor on a per Hz basis. When using a device in fractional mode, the in-band phase noise may slightly degraded, depending on the fraction and how it is expressed. For instance, if the fraction is simple like ½, then there might be a spur produced, but minimal phase noise degradation. If the fraction used is 10000000/20000001, then this may appear to increase noise floor due to a set of closely spaced fractional spurs. This fractional noise floor appears to add to the integer noise floor modeled by the term PN1Hz. Some manufacturers, such as Analog Devices, may account for this by increasing PN1Hz by a modest amount such as 1 to 3dB in fractional mode.

The term  $PN_{1/f}$  is used by Analog Devices as a 1/f noise parameter, and is provided in their datasheets. Texas Instruments refers to this same term as  $PN_{PLL_{1/f}}$ . This parameter assumes in-band noise at 10kHz is dominated by flicker, calculation using it scales that noise by output frequency relative to 1GHz and by offset relative to 10kHz. Linear Technology uses this same basic method for specification, but they eliminate the referencing to 1GHz carrier and 10kHz offset. They use the normalized 1/f noise term  $L_{M(NORM-1/f)}$ . Let us refer to this term with the simpler variable  $PN_{flicker}$  when in linear form and  $PN_{flickerdB}$  when in dB form. We convert between these using the simple relation:

**Equation 1:**  $PN_{flickerdB} = PN_{1-fdB} - 140dB$

In Part 3 a figure of merit combining the noises of the flat and 1/f terms is developed. When comparing synthesizer chips at the same charge pump current and phase detector comparison frequency, this relationship is given by:

**Equation 2:**  $IC_{nfm} = PN_{1Hz} f_L + f_{comp} PN_{flicker} \ln(f_L)$

This figure of merit is proportional to synthesizer chip induced noise power from 1Hz to bandwidth  $f_L$ , so smaller is better. This total figure of merit is used in the below table for examples of leading synthesizer IC’s.

**Table 1:** Leading delta-sigma synthesizer IC’s. Lower noise is more expensive, but lower noise combined with higher frequency is what really costs. **Note:** Texas Instruments reports no difference in broadband phase noise between integer and fractional mode, though spurs may vary. Analog Devices typically reports a difference in integer and fractional mode normalized noise, where fractional is about 1 to 3dB noisier.

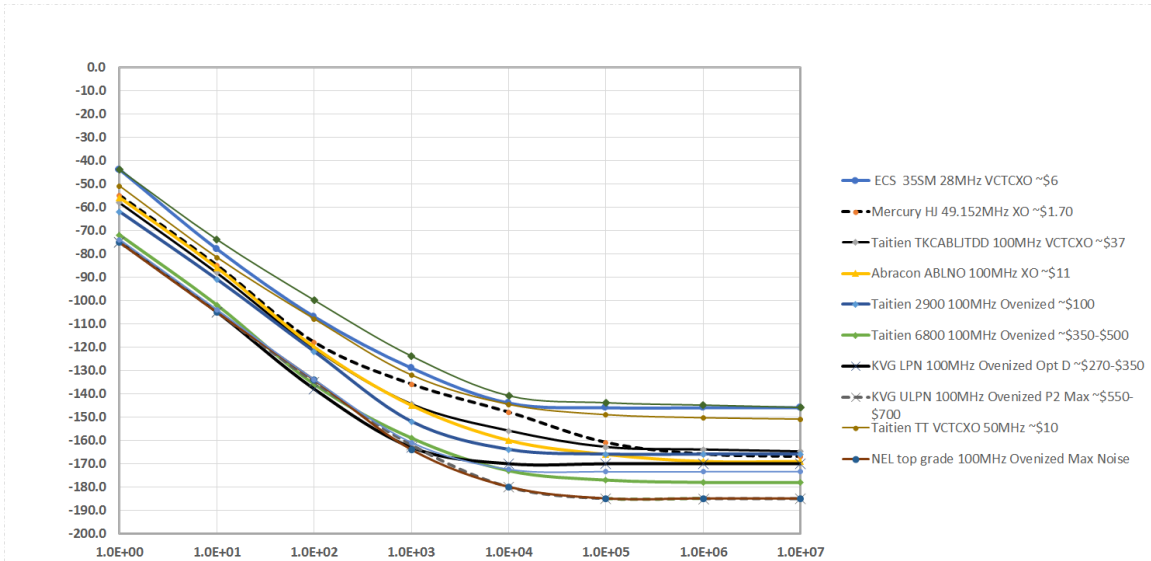
Part	Freq Range	On-Die VCO	Norm Phase Noise Floor & Flicker in dB, and total noise figure of merit	Price	Comments
TI LMX2491	500MHz to 6.4GHz	No, only ext	-227 floor dB -260 flicker dB 1.35E-17 tot	\$2.90 @1k	State of the art for the price. FMCW radar functions. Charge pump can tune to 5.25V. The LTC6947 is a similar competitor, but about 2X the

					cost. The <b>LMX2492</b> is a 14GHz version for ~\$8.75@1k.
TI LMX2571	10MHz - 1344 MHz Int VCO, 100MHz -2 GHz External VCO	Yes, option for off- die	-231 floor -260 flicker 1.23E-17 tot	\$5.50 @1k	State of the art lower power synthesizer. Ext VCO to 2GHz, but RF buffer output limited to 1400MHz. This part is ideally architected for land mobile use.
TI LMX2572LP	12.5MHz – 2GHz	Yes	-232 floor -265.5 flicker 5.77E-18 tot	\$6 @1k	State of the art lower power, lower freq, lower cost synthesizer.
TI LMX2582	20MHz – 5.5GHz	Yes	-231 floor -266 flicker 3.67E-18	\$9 @1k	State of the art for the price in a medium frequency. The <b>LMX2592</b> is a 9.8GHz version for \$20.50 @ 10k.
TI LMX2594	10MHz – 15GHz	Yes	-236 floor -269 flicker 1.7E-18 tot	\$42.50 @1k	State of the art on-die VCO synth IC. The -235dBc/Hz normalized frac PLL noise is the lowest currently available. The <b>LMX2595</b> is a 20GHz version for \$62.50 @ 1k.
Analog Devices ADF41513	1GHz – 26.5GHz	No, ext. only	-234 int floor -231 frac floor -267 flicker 3.09E-18 tot	~\$30 @1k	State of the art for a high frequency ext. VCO synthesizer. The -231dBc/Hz fractional normalized PLL noise is the lowest currently available for external VCO's.
Analog Devices ADF4372	62MHz – 16GHz	Yes	-234 int floor -233 frac floor -267 flicker 2.3E-18 tot	~\$65 @1k	Near state of the art, though LMX2594 is a direct competitor with lower noise and cost. Typical spurious -90dBc. The <b>ADF4371</b> is a 32GHz version at ~\$250 @ 1k.
Analog Devices ADF5610	57MHz to 14.6GHz	Yes	-232 int floor -229 frac floor -268 flicker 2.46E-18 tot	~\$48 @ 1k	Near state of the art at a lower price than the ADF4372, with low typical spurs of -105dBc, at the cost of about 4dB in-band phase noise.

## Crystal References

In the case of the modern delta-sigma, fractional N, high bandwidth synthesizer, the crystal reference oscillator is a critical component and can often be the most expensive component in the system. There will be an offset frequency from the carrier below which it is the multiplied crystal oscillator noise that sets the locked noise. This is crucially important in some systems.

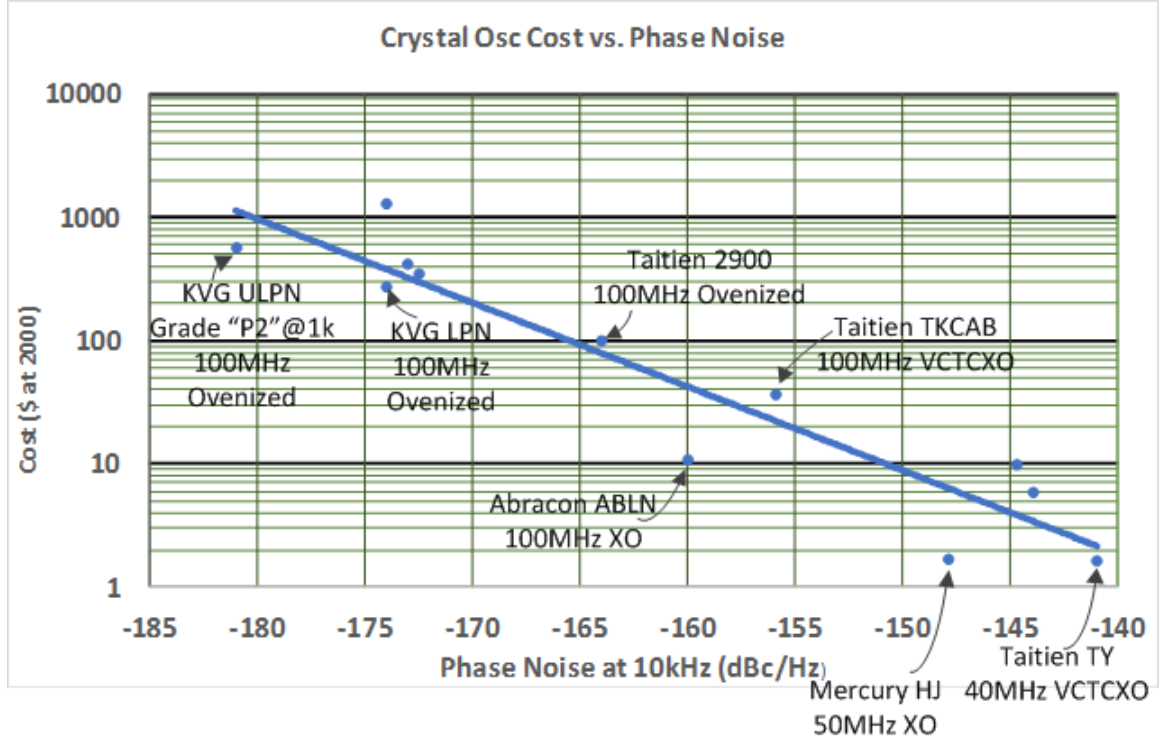
The below graph shows the phase noise performance of a set of commercially available crystal reference oscillators that under different conditions are all well suited for modern delta-sigma usage. Though these are mostly low noise oscillators for their price, there is an approximately 30 to 40dB variation in phase noise. Even more striking is the price variation, varying from less than \$2 to over \$1000.



**Figure 1:** Example phase noises for crystal oscillators of excellent noise performance. These commercially available parts are from 28MHz to 100MHz, and are here normalized to 100MHz noise performance for fair comparison. Note that there are many grades or options with crystal oscillators that can move price-performance significantly.

The “big three” specifications dictating the approximate costs are phase noise, frequency, and frequency accuracy. For decades 10MHz was the standard frequency of the finest low noise crystal oscillators, but 100MHz is rapidly becoming a new standard for this application, with both voltage controlled temperature compensated crystal oscillators (VCTCXO’s) and ovenized oscillators now available. Lower cost simple crystal oscillators will typically have 10ppm to 100ppm accuracy, which if acceptable can allow for quite good noise performance for prices ranging from less than \$2 to about \$12. Generally, VCTCXO’s offer frequency accuracy from about 0.5ppm to 2ppm (parts per million), though some ultra-low phase noise VCTCXO’s may have more error as a result of the necessary crystal cut and high power for lowest noise. VCTCXO’s at frequency under 40MHz with phase noise suitable for wireless handsets (typically consuming less than 3mA) are available for less than \$2 and in high volume sometimes less than \$1. At 40MHz and under performance suitable for base stations is about \$4 to \$8 (for example, ECS 35SM). But, newly released VCTCXO’s at 100MHz (Taitien TKCAB) that are ideal for the latest synthesizer IC’s aimed at high performance communications, wireless infrastructure, and test equipment are tending to be in the \$25 to \$40 price range. For the most demanding applications, ovenized oscillators at 100MHz with initial frequency accuracy from 0.2ppm to 0.5ppm (after typically 30 minutes warm-up), and very well controlled aging and temperature drift range, are available from about \$70 to \$1500. However, outstanding performance can be had by the careful designer for about \$250 to \$800 depending on quantity and grade (for

example, KVG LPN and ULPN). The approximate price-performance ratios now offered in the market may be visualized from the graph below.



**Figure 2:** This approximate price vs. noise performance of well performing crystal oscillators, with trend line curve fit, gives a designer a quick view of about what has to be spent to get a certain phase noise performance.

This dB linear graph shows that the general cost vs. phase noise function is an approximate hyperbola where:

**Equation 3:**  $Cost \approx \frac{a}{P_n^b}$

In this equation, a and b are positive constants and  $P_n$  is the noise power in a 1 Hz bandwidth to carrier ratio at a particular offset frequency. For the above data, with cost in dollars and  $P_n$  specified at 10kHz, an approximate curve fit shows  $a = 1E-11$  and  $b = 1.561$ . The high end of pricing publicly revealed by suppliers in support of this article is about \$700, but the author is familiar with pricing that exceeds \$1000 for some of the best available phase noise. Attaining a few dB phase noise advantage may require expensive special measures such as crystal sorting, so such prices may be justified. For applications such as the radar in a fighter aircraft, where the survival of a pilot, the preservation of a \$100M fighter plane, and consequences of a failed mission may be at stake, even higher prices may be justified.

We see above that several companies show well above average cost effectiveness, and that less accurate (neither ovenized or temperature compensated of typically ~25ppm total error) crystal oscillators can offer outstanding phase noise for their cost. A cost of at least \$10 is usually needed to get to 100MHz (Abracon ABLN).

More details of examples of good performance-price ratio crystal oscillators are reviewed in the below table.

**Table 2:** Strong crystal oscillator candidates for low noise synthesizers. Costs reflect moderate to medium volume for the typical applications of the part, and in some cases are interpolated by the author from available information. “Relaxed accuracy” is a relative term here, as in a synthesizer application in tightly specified communications systems anything over about +/-2 to 4 ppm total error is sometimes unacceptable. The relaxed accuracy references shown here offer outstanding performance for the price in situations where the best accuracy is not required.

General Requirements	Part	Freq	Accuracy and Phase Noise @ 1kHz Norm to 100MHz	Typical Cost	Comments
Low cost VCTCXO	Taitien TY	40MHz	+/-1ppm -124dBc/Hz	~\$0.80 to \$1.80	Excellent performance for a low cost handset class VCTCXO.
Low cost and relaxed accuracy up to 50MHz	Mercury HJ XO series	20 to 50MHz	25, 50, and 100ppm total error including temp. -135dBc/Hz.	~\$1.3 - \$2.90	Outstanding noise for the price. Mercury reports they can offer these parts at +/-5ppm and +/-10ppm accuracy at 25 deg C. That implies max temp drift over -40 to +85, aging, and supply can be limited to 18ppm. Standard CMOS output.
Low cost and relaxed accuracy up to 160MHz	Abracon ABLNO XO series	24.576 to 160MHz	+/-12ppm typ at room temp, additional +6 / -8ppm over -30 to +85C. -143dBc/Hz.	~\$8 - \$12	Outstanding noise for the price, if accuracy is acceptable. 28ppm max total error - 18ppm max temp drift – 7ppm aging => set on accuracy of 3ppm. Nom freq error over -40 to +85C and 10 years aging is thus 22ppm.
High performance VCTCXO	Taitien TKCAB	100MHz	+/-1ppm at 25 deg C and +/- 1ppm over temp. -145dBc/Hz	~\$30 to \$45	A new breakthrough VCTCXO within 5-7dB of the noise of low end ovenized oscillators for about 1/3 the price.
High performance VCTCXO	NEL AN-X0AU AN-XA7XU	60-128MHz, nom 100MHz	Grades ranging from +/- 0.28ppm to +/- 25ppm -155 to -160dBc/Hz	Not public	High performance VCTCXO that competes with ovenized oscillators for generally less cost and much less power.

Low end ovenized	Taitien 2900 series	100MHz	+/- 0.2ppm at 25 deg C and 50ppb over temperature. -152dBc/Hz	~\$80 to \$110	An excellent representative of the lower end of ovenized references, with outstanding accuracy.
Mid grade ovenized	KVG LPN series	80-150MHz, nom 100MHz	+/-0.3ppm at 25C 20-200ppb over temp and grade. -163dBc/Hz max	~\$350 @100 ~\$285@1k	Superior noise performance for mid-grade ovenized. Options are available from "A" to "D" that trade close in noise against far out noise. Opt D pricing is shown here.
High end ovenized	KVG ULPN series	100MHz	+/-0.3ppm at 25C 50-500ppb over temp and grade. -164dBc/Hz max	~\$700 @100 \$500 to \$750@1k over grade	High grade performance at the low end of high grade pricing. Grades P1, P2, and P3 are available, with the highest performance P3 grade being noted here.
High end ovenized	NEL O-CIH	100MHz	50ppb over temp -158 to -166 dBc/Hz over grade	Not public	State of the art in the higher grades.

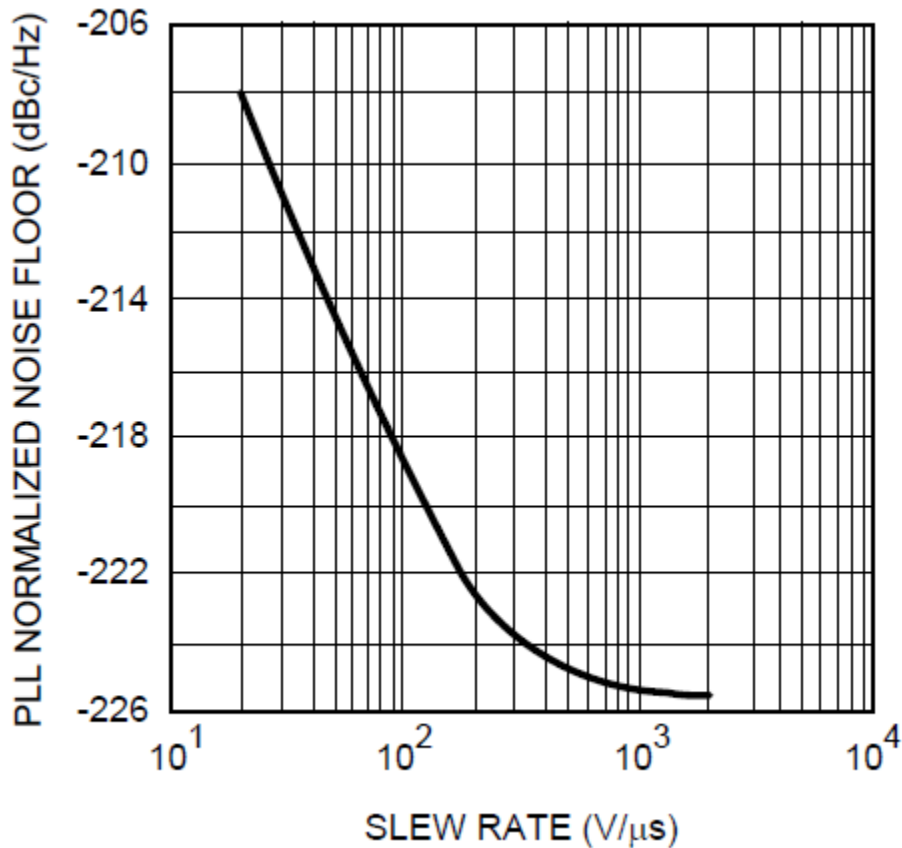
### Crystal Reference Drive and Buffering

This subject is insufficiently reported on, and often more difficult than it seems at first glance. A designer may naturally think that driving the reference inputs of the synthesizer IC is an almost transparently easy task, but that is not the case. These inputs have demanding slew rate requirements for best noise performance, may have matching requirements, and often have some surprising voltage requirements. A voltage peak to peak swing above a minimum is needed, but usually also with a maximum that is less than the synthesizer chip supply rails. For example, a typical range for various modern synthesizers with a 3.3V supply is a minimum somewhere from 0.2Vpp to 0.5Vpp and a maximum somewhere from 2.0 to 3.3Vpp. These voltages may significantly differ between single ended and differential. Getting the right voltage swing tempts a designer to use resistive padding, which may be of lower impedance than a CMOS output is specified to drive, and which will slow down the slew rate and increase noise as discussed below.

Though described in the data sheets of only a small number of synthesizers, some data sheets do note the potentially large negative impact of slower crystal reference rise and fall times on the closed loop noise. This noise applies to both the flat and 1/f noises of the charge pump and dividers, which is commonly referred to as "PLL noise" (see Ref. 3, article 3 of this series).



According to some recent Texas Instruments data sheets, noise increases exceeding **15dB** can occur from this source, such as shown below.



**Figure 3:** Texas Instruments LMX2541 data sheet relationship between normalized noise floor and crystal reference  $dv/dt$ . A similar graph applies to  $1/f$  noise degradation. It is not specified in the data sheet if this applies to differential input or the optional single ended input. If differential and for each input, which seems likely from the test set ups shown in the data sheet, then single ended input would presumably need twice the  $dv/dt$  for the same noise performance.

Many ovenized oscillators provide only a slower sine wave output, which is probably a result of them being specified as able to drive a 50 ohm load. This tends to work out fine for 100MHz, but not for the other common frequency of 10MHz. For example, at 100MHz, with 3Vpp swing into 50 ohms, the maximum  $dv/dt$  (over the sine wave) is 940 V/μs (based on  $dv/dt(\max) = Vp\omega$ ). To read normalized PLL phase noise when only single ended, the correct phase noise would be read for half this  $dv/dt$ , thus effectively 470V/μs in terms of using the graph above. That is apparently a single ended degradation of about 1dB on the LMX2541 graph. But, a 10MHz ovenized oscillator would have effective slope of only 47V/μs, and thus on the LMX2541 graph a phase noise degradation of about 11dB.

Crystal oscillators often have the option of higher speed CMOS outputs that reduce this problem significantly for lower frequency oscillators, as least as compared to sine wave or clipped sine

wave outputs. If we take the above graph as typical, containing this degradation within 1dB requires differential  $dv/dt$  on the order of about  $400V/\mu s$ , or single ended  $dv/dt$  of about  $800V/\mu s$ . Taking 3V as the typical swing of a CMOS crystal output, and allowing for the typical 10% to 90% rise time specification, that takes a rise time of 3ns. Some parts guarantee that, such as the 3ns max rise time of the Taitien TKCAB 100MHz VCTCXO. But, others may have maximum rise times on the order of 10ns (worst case Mercury HJ), which is  $240 V/\mu s$  single ended or  $120V/\mu s$  equivalent differential. On the above probably differential graph this is about 7dB of degradation.

We see from typical data sheets that full awareness of this degradation appears to be a recent enough development that not all crystal oscillator providers have yet provided sufficiently high  $dv/dt$  and drive on their CMOS outputs to totally avoid this problem. Drive limitations occur because crystal oscillators typically specify their drive into high impedance loads. For example, the Taitien TT type VCTCXO is specified to drive its CMOS output into 10k in parallel with 10pF. The higher power and lower noise Taitien TKCAB VCTCXO, a ground breaking device that fills a major hole in the market between standard VCTCXO's and low end ovenized oscillators, is specified as able to drive 1k in parallel with 15pF, and still have a maximum rise time of 3ns. Some others specify no resistive load capability at all.

The crystal drive problem can be further exacerbated by the advice given in some synthesizer data sheets. There is a tendency to recommend supporting clock distribution by brute force matching with 50 ohm single ended resistors in parallel with high impedance synthesizer reference inputs, or 100 ohms across a differential drive (effectively 50 ohms each). While this may be fine for high frequency ovenized oscillators with their high power sine wave outputs, CMOS outputs typically are not specified to drive such low impedance. They are not guaranteed to meet their specs on rise time into lower impedances, and when higher impedances are created by series padding they suffer RC slew rate reduction. Naturally a designer does not want to pay for a high quality crystal oscillator only to waste its low noise performance due to this drive problem.

One solution that is sometimes recommended is crystal oscillators with LV-PECL outputs (low voltage positive emitter coupled logic). This is a differential current steered output form, able to drive 50 ohms, with peak to peak swing on each channel of about 0.8V, and rise/fall times of about 1ns max. ECL was invented to distribute high speed clocks and it is good for that purpose. But, such oscillators generally consume 50mA to 100mA, and the  $dv/dt$  is about  $0.8V/ns$  for each channel and  $1.6V/ns$  effective differential. So, it's about half the recommended  $dv/dt$ , and with a large current consumption that is overkill just to drive a high impedance synthesizer input.

The following is recommended instead when working with CMOS outputs. First, use sufficient  $dv/dt$  by use of a crystal oscillator with built-in high  $dv/dt$  or by use of a fast, low noise buffer. Second, routing distance from driver to synthesizer reference input can be kept sufficiently short that there is not a need to brute force match the line with 50 ohms or other low impedance that may reduce voltage and  $dv/dt$ . Third, the drive can be differential, effectively doubling the slew rate.

This clock buffering and squaring operational need for both distribution of clock signals and increasing  $dv/dt$  has not gone unnoticed by the semiconductor companies. There are a number

of clock buffer chips on the market, several of which are excellent for use with synthesizer reference inputs.

Linear makes a fast, very low noise buffer, the **LTC6957**, which can drive single ended or differential with very fast rise and fall times of typically 0.17ns. However, it requires a 3.3V supply, so it usually requires padding to bring its voltage down within the synthesizer's typical input range, thus slowing its slew rate. At about \$4 it is also a fairly expensive part for some applications. A slightly greater than \$1 part that may serve well despite somewhat higher noise than the LTC6957 is the Texas Instruments **CDCLVC1102**. Its two outputs are ideal for differential drive. This part also comes in higher fanout versions if it is desired to distribute the crystal output for other uses. Or, for even lower cost, CMOS inverters and appropriate supply levels and moderately loaded padding may serve, though they will be somewhat higher noise than the purpose designed low noise buffers listed above. As their noise levels are undocumented, they need to be measured on a phase noise test set confirm their acceptability.

There is a disconnect here in the market between optimum drive for different synthesizers and what crystal oscillators typically provide. Until such time as the crystal makers provide fast, low jitter, voltage adjustable, and selectable single ended and differential drive, synthesizer designers will have to provide this function themselves. This may require a careful reading of the particular data sheet, and careful simulation of the drive circuitry used to interface from the crystal oscillator to the particular synthesizer IC.

### **Discrete Voltage Controlled Oscillators**

In the early years of PLL synthesizers, many designers developed their own discrete VCO's. However, the challenge of developing really low noise VCO's soon led to high performance VCO design becoming the specialty of RF module design houses. These companies were specialists in pushing Leeson's Equation (Ref. 2) to the limits of physics and parts, which required high Q resonators and a detailed understanding of all the noise sources in a VCO. Many of these design techniques are hard won, and are not made public. Over several decades of development, highly optimized designs resulted. To remain relevant with on-die VCO's taking an ever-increasing market share, new even lower noise VCO's have continued to come out, such as the narrowband VCO's offered by Mini-Circuits, Synergy Microwave, Z-Comm, and Analog Devices. The best narrowband VCO's have about 10 to 30 dB better noise performance than the best on-die VCO's. Synergy Microwave, with their metamaterial resonator VCO's, offers octave bandwidth VCO's with phase noise that is within about 5dB to 20dB of the best narrowband VCO's at similar frequencies, and typically about 2dB to 8dB superior to the finest on-die VCO's. However, the best on-die microwave VCO's at frequencies above about 4GHz, by using multiple VCO's and hundreds of narrowband resonators, are able to often match or beat the far out noise of octave bandwidth discrete VCO's. Though on-die VCO's are probably taking over 80% of design-ins, high performance discrete VCO's are still finding application in microwave links, test equipment, military communications, and wireless infrastructure. Some key examples are given in the table below.

**Table 3:** Noteworthy VCO candidates for low noise synthesizers. While noise well inside the PLL bandwidth will be similar to that of integrated VCO's, these parts can provide significantly lower phase noise around and past the loop bandwidth.

<b>Part</b>	<b>Freq</b>	<b>PN @ 10kHz and 100kHz, dBc/Hz</b>	<b>Tune and supply</b>	<b>Comments</b>
Synergy DCRO178205-10	1785-2060MHz	-109, -131	0.5-12V 10V@35mA	Near the limit of available for a 2GHz part with +/-7% tune range. About 13 dB better noise than the best on-die VCO performance such as that on the LMX2495.
Synergy DCYS100200-12	1GHz – 2GHz	-106, -128 (Some variation over this wide band)	0.5-28V 12V@40mA	Superb for a microwave octave tune range that with on-synthesizer dividers can hit any frequency from HF to 2GHz. About 8dB superior to a state of the art on-die VCO.
Synergy DCYS200400P-5	2GHz – 4GHz	-93, -116	0.5V-18V 5V@60mA	Excellent for an octave at this frequency, though on a normalized based about 6 dB inferior to DCYS100200-12. About 2dB superior to a state of the art on-die VCO such as that on the LMX2495. Above 4 GHz it is difficult to find octave VCO's that are significantly better than the best integrated.
Mini-Circuits MOS-975-119+	900-975MHz	-114, -135	1-9V. 5V@40mA.	Excellent for the +/-4% tune range, effectively -120 if divided by 2 to land mobile band. About 11dB superior to best on-die VCO's. \$15.75 @ 100.
Mini-Circuits ROS-1770-1PH19+	1710-1800MHz	-111, -132	0.5-8V. 5V@30mA.	Excellent for its +/-2.6% tune range, effectively -123 divided by 4 to land mobile. About 13dB superior to best on-die VCO's. \$19.95 @ 100.
Mini-Circuits ROS-2001C-119+	2GHz (1997-2003MHz)	-126, -147	0.5-9.5V. 8V@38mA.	Excellent for pure performance at 2GHz, even though a point frequency product. About 29dB better than best on-die VCO's. \$39.95 @ 50.
Z-Comm ZRO0915C2LF	902-928MHz	-128, -147	0-11V. 10V@23mA.	Superb for 902-928MHz low noise apps such as RFID readers. About 23dB better than best on-die performance. Budgetary pricing ~\$19 for 1k and \$13 for 10k.
Analog Devices HMC510	8.45-9.55 GHz	-92, -116	2 – 13V 5V@315mA	Excellent noise in this narrowband family for frequencies in the range of 8 to 27GHz. This particular VCO is about 11dB better than the best on-die VCO's at 100kHz, and others in this family in the range of 8-12dB better. These have div by 2 outputs and some

				also div by 4 in order to use lower cost, lower frequency synthesizer IC's. \$22.55 at 50.
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## Power Supplies

An area of important recent advance has been that of low noise regulators. Noise on supplies will directly modulate noise on a VCO, as described in article 2 of this series. As recently as 2010 a noise floor of about 10 to 30 nV per root Hz was considered as “ultra-low noise”. These levels could induce considerable degradation of the phase noise of a low noise VCO. Lower noise regulators were then introduced to the market, but up to 2015, noises in the range of 3nV to 15nV were considered ultra-low noise. For this reason, the author had previously designed custom discrete regulators with floor of 1nV or lower when such performance was needed. In 2015 noises as low as 2nV were introduced to the market by Linear Technology in very convenient form. For the majority of applications, a supply noise level of 2nV per root Hz eliminates supply noise as a practical concern.

Noise modulated from VCO supply to VCO output in the unlocked state was given in Part 2 as:

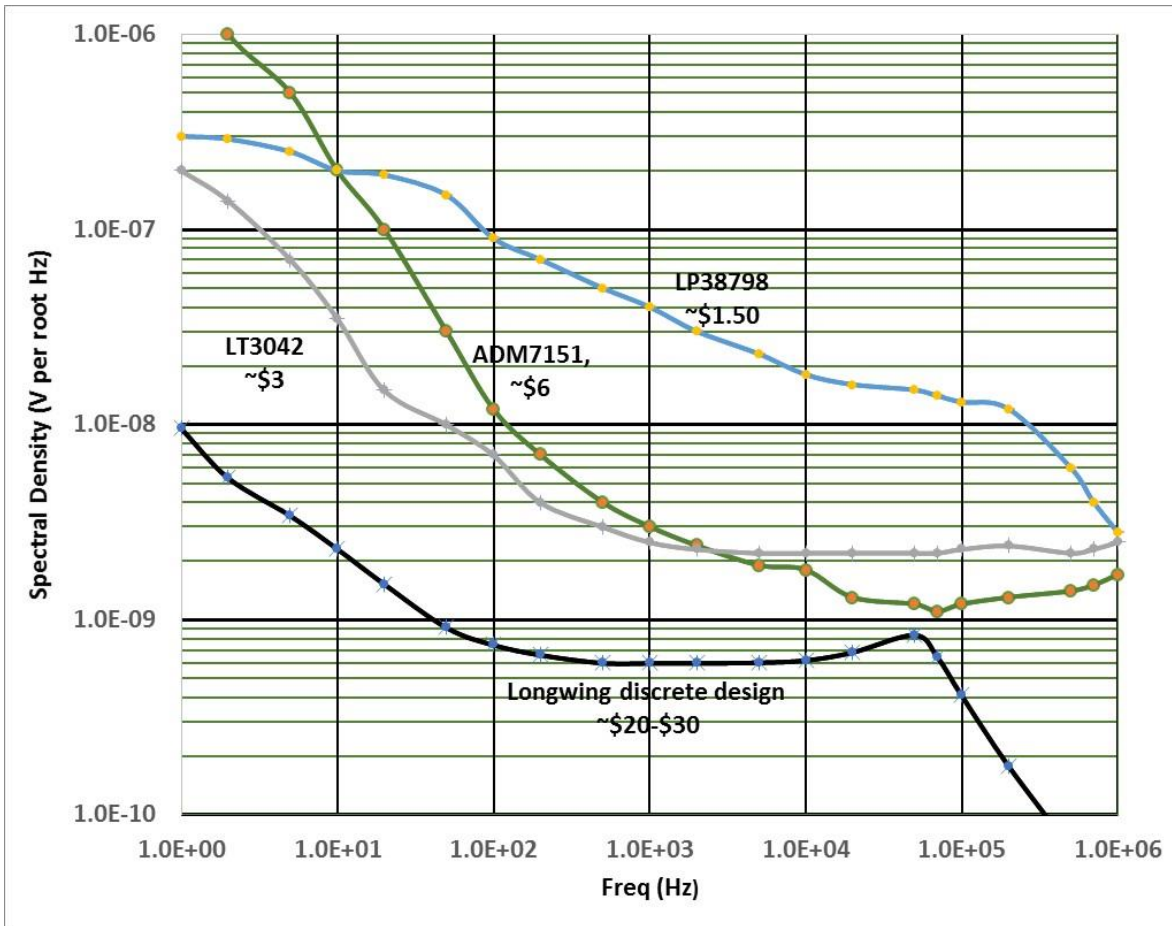
$$\text{Equation 4: } \frac{S}{C} (\text{power supply}) = S_{cp} = \frac{V_{np} K_p \text{Hz}}{\sqrt{2} f}$$

We see that for both input and power supply noise that a frequency flat noise spectral density will cause phase noise to decline at 20 dB/decade as frequency increases. Over this range of frequency, a constant (over frequency) allowed noise density on steering and power nodes may be specified that keeps induced noise below the VCO free running phase noise on the most important 20dB/dec part of the phase noise curve. The VCO input noise  $V_{n1}$  will include PLL loop filter noise. With switching regulators, the suppression required to reduce the power supply noise  $V_{np}$  to negligible can exceed **100 dB**. Such high noise suppression will generally require at least one active linear regulator stage plus passive filtering, and may require two active stages. This applies similarly to crystal oscillators, especially at frequencies within an order of magnitude of the modulation bandwidth of the crystal oscillator.

Regulator noises for four top options are shown below. While the Analog Devices ADM7151 is to the author’s knowledge the lowest noise floor integrated regulator on the market, its 1/f noise is not the best, and its output is limited to 5.1V. In the author’s opinion, the most usable low noise regulator on the market is the 2nV floor Linear Technology (now Analog Devices) LT3042. This part is based on the simple expedient of strongly filtering a variable voltage reference, and then following that with a unity gain power buffer that does not gain up noise or introduce resistor noise. It provides voltages of 0 to 15V at up to 200mA out, and the new LT3045 provides up to 500mA. The also recently introduced LT3093 and LT3094 provide similar performance in negative voltage regulator form--a long neglected hole in the market for ultra-low noise negative regulators that is now finally filled. In addition to their low noise that satisfies most system requirements, the advantages of these regulators include single resistor programming of voltage, low drop out, high power supply rejection ratio, a “fast lock” feature, a low enough value of reference bypass capacitance to use high dielectric constant ceramic capacitors, or film capacitors

when high vibration immunity is needed, and the ability to parallel the regulators. The paralleling feature may seem like a marketing tactic to sell more chips, but it actually has high value. Not only can it provide higher power and current capacity while often avoiding the use of heat sinks, but it reduces noise power in inverse proportion to the number of units paralleled. For example, paralleling two units will reduce noise power by 3dB, thus reducing noise floor from about 2.1nV to 1.5nV per root Hz.

If an application demands lower 1/f and floor noise than a reasonable paralleling of LT30XX family members can provide, then an option is a discrete low noise regulator. This more expensive method can provide noise floors well below 1nV, and 1/f noise voltage approximately 20-25dB lower than the finest integrated regulators.



**Figure 4:** Ultra-low noise regulator available spectral noise density. The LT3042 and ADM7151 noise curves are both with 22µF noise filter capacitances.

**Table 4:** Key specifications of several top low noise regulator choices.

Regulator	Key Specs	Cost and Comments
TI LP38798	$V_{in}$ 3V to 20V $V_{out}$ 1.2 to $V_{in}$ -Dropout Current limit 800mA	~\$1.50 at 2k distributor. Noise is first order independent of output voltage.

	Dropout 200 mV Thermal resistance ~35degC/W	The low cost choice for a low noise, high current, high voltage regulator.
Linear LT3042 (200mA) LT3045 (500mA) LT3093 (200mA neg) LT3094 (500mA neg)	V <sub>in</sub> 1.8V to 20V V <sub>out</sub> 0 to 15V Current limit 200mA Dropout 350mV Thermal resistance ~33degC/W	~\$2.85 at 2500 distributor. Noise is first order independent of output voltage. The ultra-low noise choice for wide voltage range, and positive and negative outputs in same family.

### Low Noise Op Amps

Op amps are needed for boosting charge pump outputs to the higher voltages needed for tuning the very finest discrete VCO's. However, their noise will directly modulate noise onto the VCO output, and must be very low to be transparent (Ref. 2). Op amps with noise floors approaching 1nV have been available for many years, but in recent years these op amps have improved with lower input current (important for low spurs) and current noise (also very important), greater common mode range, and higher bandwidth (important to spurs and phase shift). However, the very lowest noise op amps are not rail to rail, and care must be taken with the locking of the PLL using these op amps. Typical methods of working with non-RR op amps are to make use of a low noise negative supply for the op amp, pre-charge the loop filter under software control to be within the input voltage range of the op amp, or switch in a rail to rail op amp during initial settling.

**Table 5:** Low noise op amps for use in low noise synthesizers. The shorthand W-X-Y-Z here refers to spectral noise density (voltage or current) at frequencies spaced a decade apart, usually starting at 1Hz.

Op Amp	Major Specs	Cost and Comments
TI OPA209 single and OPA2209 dual	Rail to rail output, 1.5V drop on input. Voltage noise 8.1(1Hz)-3.3-2.3-2.2-2.2 nV. Current noise 1.6pA (1Hz)-0.6-0.5-0.5. Supply 4.5 to 36V. Input bias 1nA to 8nA. 18 MHz GBW.	Single \$1.10 @ 1k Dual \$1.65 @ 1k Lower input bias and noise current than most ultra-low noise op amps can sometimes enable outperforming op amps with lower voltage noise.
TI OPA1611single and OPA1612 dual	Output rail to rail, input from V <sub>ss</sub> +2 to V <sub>cc</sub> -2V. 1 Hz to 10 kHz voltage noise of 7-3-1.5-1.2-1.1 nV per root Hz. Current noise 11pA (1Hz)- 4.5-2.9-2.7-2.7. Supply 4.5V to 36V. Input bias 60 to 350 nA. 40-80 MHz GBW.	Single \$1.75 @ 1k Dual \$2.75 @ 1k Outstanding noise performance, current noise is about 5X the OPA209, but much lower than competing Max9632. The OPA211 is a more expensive version with better input voltage limits.

TI LMP7731(single) and LMP7732(dual)	Rail to rail input and output. Voltage noise 4.2(1Hz)-3.1-3.0-2.9nV. Current noise 8pA(1Hz)-3-1.2-1.1pA Supply 1.8 to 5.5V, input bias 1.5 to 50nA. 22MHz GBW.	Single \$0.63 @ 1k Dual \$1.05 @ 1k Lowest noise RRIO part that TI has. The competing Linear LT1678 dual RRIO has noise of 7.5(1Hz)-4.5-4.0-3.9 nV.
Linear LT1677	Among lowest noise RRIO op amps with higher voltage. Voltage noise 18(1Hz)-5.2-3.3-3.2nV. Current noise 1.2pA(10Hz)-0.4-0.3. 3V to +/-18V supply, ~3mA. 7.2MHz GBW.	~\$2.80 @ 1000 distributor. LT1678 is a similar dual version, ~\$3.15 @ 1000 distributor. Suitable for low noise (not ultra-low noise) single op amp loop filters where its rail to rail performance simplifies circuit design of locking problems that unassisted non-RR op amps may suffer.
TI OPA2156	Dual low cost low noise high voltage RR op amp. Voltage noise 150(1Hz)-40-11-4-2.9nV. Current noise 19fA at 1kHz. 4.5V to 36V supply, ~4.4mA. 25MHz GBW.	First of a new family, single op amp versions likely to follow. Dual: \$1.25 @ 1k. High 1/f corner ~700Hz, but this can be suppressed by a wideband synthesizer. Suitable for single op amp loop filter with op amp to spare.
TI LM7321 LM7322	RR input and output. Noise 100 (1Hz)-40-18-15 nV. 2.5V to 32V supply, 1.3mA. 20 MHz GBW.	Single: \$0.71 @ 1k Dual: \$0.97 @ 1k Suitable as a low cost rail-rail op amp for settling the active filter prior to switching in an ultra-low noise non-RR op amp.

## Summary

Delta-sigma synthesizer IC's with on-die VCO's and output dividers have reshaped the design of synthesizers in the last decade. Available to frequencies as high as 32GHz in 2019, they can typically provide any output frequency from a few tens of MHz to their upper frequency limit. The inherent higher phase noise of on-die VCO's has been partially tamed by switching VCO's and resonators for the best open loop on-die VCO phase noise, and then suppressing that noise with high frequency crystal oscillators and higher phase detector frequencies allowing higher loop bandwidths out to approximately 200kHz to 400kHz. Discrete VCO based synthesizers can still offer the advantage of superior phase noise around and past the loop bandwidth. For the best narrowband and point frequency VCO's, this advantage is quite significant, at about 20 to 30dB. For octave bandwidth VCO's that offer similar frequency flexibility to on-die VCO's, the advantage is more limited, at about 2dB to 8dB for frequencies below 4GHz (an little if any current advantage above 4GHz except in narrowband form). The discrete VCO approach currently pays a penalty of moderately higher noise (~3-4dB) over part of the range within the loop bandwidth due to the best PLL noise (charge pump and divider noise) being available only for VCO on-die synthesizers and not for synthesizers supporting external VCO's. The discrete VCO approach also requires extra parts for higher voltage supplies and active loop filters. Still,



in markets like test equipment, microwave links, wireless infrastructure, and low noise communications where noise around and beyond the loop bandwidth is important, there are places for the discrete VCO approach. Examples will be shown in the concluding 5<sup>th</sup> article of this series.

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## Article 4 References

1. "Design Methods of Modern Ultra-Low Noise Synthesizers," Farron Dacus, *Microwaves & RF*, Dec. 2018.
2. "Noise Sources in Ultra-Low-Noise Synthesizer Design", Farron Dacus, *Microwaves & RF*, Feb. 2019.
3. "Noise and its Shaping in Ultra-Low-Noise Synthesizer Design", Farron Dacus, *Microwaves & RF*, Mar. 2019. Long forms of these articles with more detail are posted at [www.longwingtech.com](http://www.longwingtech.com).
4. "Supply clean power with ultra-low-noise LDO regulators", Steve Knoth, [https://www.electronicproducts.com/Power\\_Products/Power\\_and\\_Control/Supply\\_clean\\_power\\_with\\_ultra\\_low\\_noise\\_LDO\\_regulators.aspx](https://www.electronicproducts.com/Power_Products/Power_and_Control/Supply_clean_power_with_ultra_low_noise_LDO_regulators.aspx)
5. "A 2-to-16GHz BiCMOS  $\Delta\Sigma$  Fractional-N PLL Synthesizer with Integrated VCO's and Frequency Doubler for Wireless Backhaul Applications", Tino Copani et. al., STMicroelectronics, 2016 ISSCC. Available from the IEEE.