Design and Optimization of Frequency Modulated Phase Locked Loops

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The phase locked loop is currently the dominant method of frequency synthesis, and will probably remain so for years to come. However, it does have a few weaknesses, such as the difficulty in accurately and smoothly frequency modulating its output. This article will present analysis and design techniques for frequency modulated phase locked synthesis. Though highly useful and relatively easy to develop, these fundamental techniques do not seem to be widely known.

The method presented here, which shall be referred to as the FM PLL, involves summing a modulating signal into the loop control voltage. This method allows wide bandwidth and smooth modulation, but is not without problems. Most of the problems revolve around the loop's tendency to resist the modulation as an undesired error, resulting in unacceptable distortion. An elegant solution to this problem has been described in a previous *RF Design* article (1). Practical design and optimization methods will be presented here.

Normalized Form PLL Analysis

In control systems analysis, and particularly for second order control systems, a standard normalized form for the expression of transfer functions and time domain responses has evolved. Use of this form is extremely convenient for the design of the standard second order PLL, but the common references do not discuss its application to the FM PLL. It turns out that the normalized form is easily extendable to the FM PLL and leads directly to the development of a straightforward design procedure. Let us briefly review it as it applies to the standard PLL. Please refer to Figure 1 for the following discussion.

The PLL is nothing more than a control system. In a control systems sense, the voltage controlled oscillator (VCO) functions as an integrator from input voltage to output phase. It is the output of this integrator that is controlled and, because frequency is by definition the time derivative of phase, the frequency is also controlled. The output frequency is forced to be $N\omega_{ref}$.

In PLL analysis, the steady state output (carrier) may be viewed as a DC operating point. Our interest is in understanding the small signal AC behavior of the loop in response to outside stimuli, such as modulation. The analysis may be carried out in the frequency domain. Though it can be confusing, it is just as valid to analyze frequency variation in the frequency domain as it is to analyze voltage variation in the frequency domain.

Several transfer functions are of interest. The phase transfer function is defined as:

$$H(s) = \frac{\theta_2(s)}{\theta_{ref}(s)} \quad (1)$$

The phase transfer function may be obtained in terms of specific loop variables by solving for it in terms of the relationships defined in Figure 1. This process shall be termed substituting around the loop. The result is:

$$H(s) = \frac{K_d K_o F(s)}{Ns + K_d K_o F(s)} \quad (2)$$

Equation 2 may be placed into normalized form when an explicit form is substituted for the loop filter function F(s). For frequency synthesis applications, the most common filter form is the type 3 active filter (2). This low pass filter acts as an integrator at low frequencies, with a higher frequency zero that prevents loop instability by keeping its phase shift less than 90 degrees. Circuits for this filter are shown in Figure 2. Analysis of the type 3 active loop filter yields its transfer function to be:

$$F(s) = \frac{-(1 + s\tau_2)}{s\tau_1} \quad (3)$$

where:

$$\tau_1 = R_1 C_1 \quad (4)$$

$$\tau_2 = R_2 C_1 \quad (5)$$

It is common in the literature to ignore the negative sign in equation 3, and leave it to the circuit designer to get the

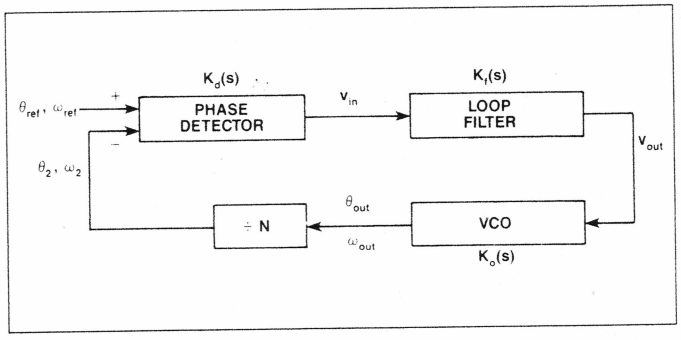

Figure 1. The basic phase locked loop.

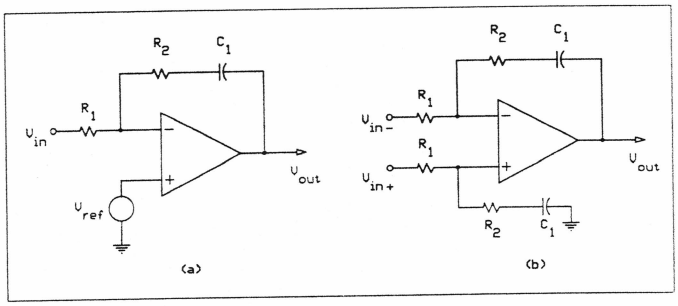

Figure 2. The type 3 active loop filter, a) Single ended input, b) differential input.

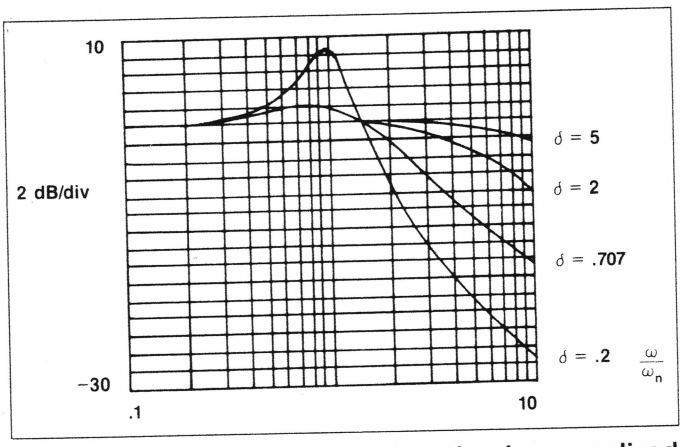

Figure 3. The phase transfer function in normalized form.

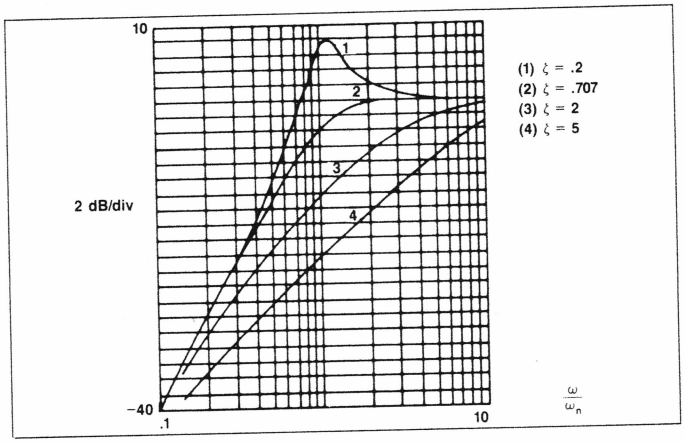

Figure 4. Curves of H (s).

signs right in the hardware to ensure negative feedback. Dropping the negative sign and substituting equation 3 into equation 2 yields:

$$H(s) = \frac{\frac{K_o K_d}{\tau_1 N}(1 + \tau_2 s)}{s^2 + \frac{K_o K_d \tau_2}{\tau_1 N} s + \frac{K_o K_d}{\tau_1 N}} \quad (6)$$

We are now ready to convert to the normalized form. In control theory, the standard normalized form of a second order equation is written as:

$$s^2 + 2\zeta\omega_n s + \omega_n^2 \quad (7)$$

In equation 7, ζ is referred to as the damping factor, and ω_n as the natural frequency. Equating coefficients between this equation and the denominator of equation 6 shows that the denominator can be expressed in normalized form if the following definitions are made.

$$\omega_n = \sqrt{\frac{K_o K_d}{\tau_1 N}} \quad (8a)$$

$$\zeta = \frac{\tau_2 \omega_n}{2} \quad (8b)$$

Subsituting equations 7 and 8 into equation 6 yields:

$$H(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (9)$$

A MathCAD generated set of plots of this low pass function is shown in Figure 3 below. The case $\zeta < 1$ is referred to as underdamped, and the case $\zeta > 1$ as overdamped. The case $\zeta = \sqrt{2}$ is the most common design choice, as it affords the fastest recovery from transient conditions, and is near optimal for loop suppression of oscillator noise (2). The frequency $\omega = \sqrt{2} \times \omega_n$ is referred to as the loop bandwidth.

Another important transfer function is the error transfer function, $H_e(s)$, defined as:

$$H_e(s) = \frac{\theta_{ref}(s) - \theta_2(s)}{\theta_{ref}(s)} \quad (10)$$

Solving for this function and converting to normalized form gives:

$$H_e(s) = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (11)$$

Note that the error transfer function is generally high pass, so that phase error is only allowed to exist above the loop bandwidth. A family of error transfer curves is shown in Figure 4.

Analysis of the FM PLL Using the Normalized Form

With a basic understanding of the normalized form of PLL analysis, we are ready to apply it to the FM PLL. Because we only modulate the PLL in the locked condition, the analysis is of small signal quantities. This will be emphasized by use of the prefix Δ. Since the reference frequency is fixed in the FM PLL system, the small signal component of the reference signal is zero. This allows the reference to be dropped from the block diagram of the FM PLL in Figure 5.

We are critically interested in the transfer from the modulating voltage ΔV_m to the output frequency variation $\Delta\omega_{out}$. Let us define this as the frequency modulation transfer function $H_{fm}(s)$.

$$H_{fm}(s) = \frac{\Delta\omega_{out}(s)}{\Delta V_m(s)} \quad (12)$$

Solving for this function and applying the normalized form yields: (13)

$$H_{fm}(s) = \frac{K_o s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} = K_o H_e(s)$$

Like phase error, the loop will only allow modulation to exist above the loop bandwidth. The effects of ω and ζ may be further clarified by the definition of a new figure of merit, the signal to distortion ratio. The definition is arrived at by noting that the ideal FM transfer function is simply K_o. Any loop modifications to this are undesired, and all such modifications appear in the loop filter output, so a sensible definition is:

$$\frac{\text{signal}}{\text{distortion}}(s) = \left|\frac{\Delta V_m(s)}{\Delta U_f(s)}\right| \quad (14)$$

Solving for this transfer function and comparing to the phase transfer function shows that:

$$\frac{S}{D}(s) = \frac{1}{H(s)} \quad (15)$$

Since the signal to distortion may be visualized as an upside down graph of H(s), the effects of ω_n and ζ are clear. A smaller ω_n gives better signal to distortion at any frequency above the loop bandwidth, which was to be expected. However, it is also noted that for frequencies above the loop bandwidth we also get better signal to distortion for a smaller ζ. Most engineers would not have intuitively expected a strongly underdamped loop to have any advantage.

We may conclude that the smallest ω_n and the smallest ζ that are consistent with other system requirements should be used. However, for a small ζ, the designer must be careful about instability.

SPICE Modeling of the FM PLL

The validity of these results may be checked with a SPICE model. For this demonstration, an arbitrary PLL with a carrier frequency of 300 MHz and an ω_n of 1 kHz was chosen. The VCO was given a typical tuning range of 10 MHz over an 8 Volt tuning range. The phase

detector is assumed to be a type 4 digital PD with gain $V_{cc}/2\pi$. V_{cc} is assumed to be 5 Volts. If the reference is assumed to be 10 MHz, then the divide ratio N is 30. A SPICE circuit representing this system is shown in Figure 6.

The integrating action of the oscillator is created by the controlled current source E_{osc} and capacitor C_{osc}. The gains of the divider and the phase detector have been combined into the controlled voltage source E_{nkd}. The resistors R_{dum1} and R_{dum2} satisfy the SPICE DC requirements.

A set of transient simulations was run using the damping factors shown with a 10 kHz, 40 mV square wave V_m. The results, shown in Figure 7, support the conclusions just presented.

The Integrator Error Corrected PLL

A fundamental improvement to the FM PLL is described in Reference 1. The working concept is simple but ingenious. If a voltage opposite in sign but equal in magnitude to the modulation induced phase error is summed into the phase detector output, the loop will be prevented from responding to the modulation. Because the VCO acts as an integrator from input voltage to output phase, the proper function is a scaled inverting integration of the modulating voltage. The system is shown in Figure 8. Solving for the FM transfer function yields:

$$H_{fm}(s) = \frac{\Delta\omega_{out}(s)}{\Delta V_m(s)} = \frac{K_o \left(1 + \frac{F(s)K_i}{s}\right)}{1 + \frac{F(s)K_oK_d}{Ns}} \quad (16)$$

We note that if,

$$K_i = \frac{K_oK_d}{N} \quad (17)$$

then equation 16 reduces to,

$$H_{fm}(s) = K_o \quad (18)$$

Equation 18 represents the ideal FM PLL behavior. Unfortunately there are circuit errors, mostly the variation in K_o over its tuning range, that degrade the necessary match condition (equation 17). However, a very significant performance improvement can still be attained. Even DC modulation is possible, though the integrator and phase detector must be periodically reset, as described in Reference 1.

The effects of mismatch may be quantified by the definition of a new term, the integrator mismatch error, as shown in equation 19.

$$\varepsilon_i = K_i - \frac{K_dK_o}{N} \quad (19)$$

Now the signal to distortion ratio for the corrected FM PLL is shown to be:

$$\frac{S}{D}\,(\text{corrected}) = \frac{K_dK_o}{N\varepsilon_i}\frac{S}{D}\,(\text{simple}) \quad (20)$$

If the VCO gain can be precisely controlled, then the signal to distortion can be made very high at all modulating frequencies. If such control is not possible, then loop parameter optimization becomes important. The smallest possible ζ and ω_n would be used to minimize loop distortion beyond the loop bandwidth. If the system must be modulated within the loop bandwidth, then a more normal ζ of 0.5 to 1.0 would be appropriate.

Limitations of the Error Corrected FM PLL

There are several potential problems to guard against in the design of the corrected FM PLL. Among these are the effects of practical integrator performance, maintaining lock under strong modulation conditions, and prevention of unacceptable sideband levels under modulation.

Integrator drift may be curtailed by limiting the DC gain of the integrator by placing a large value resistor in parallel with the integrating capacitor. This moves the integrator pole from zero to a low frequency we shall label ω_p. We shall refer to this as the bypassed integrator. It may be shown (4) that this system will have minimum distortion and $H_{fm}(s) = K_oC(s)$ when the modulation is coupled into the VCO through the highpass function in the equation below.

$$C(s) = \frac{s}{s + \omega_p} \quad (21)$$

Another potential problem is for the phase error to reach a magnitude where the phase detector exceeds its usable range. Because the correcting integrator prevents the loop from responding to the modulation induced phase error, it may be written by inspection that the phase error is:

$$\theta_e(t) = \int_0^t \frac{K_oV_m(t)}{N}\,dt \quad (22)$$

The system will maintain lock so long as the maximum phase error is kept within the limits of the phase detector. For example, for the type 4 digital phase detector (PD), this limit is $\pm 2\pi$. A useful special case of equation 22 that is handy for a quick check is that of a simple rectangular pulse of modulation. A problem familiar to all designers of high performance synthesizers is the maintenance of adequate spectral purity. A major contributor to unwanted spectral components is the digital phase detector. The classic type 4 PD represents the

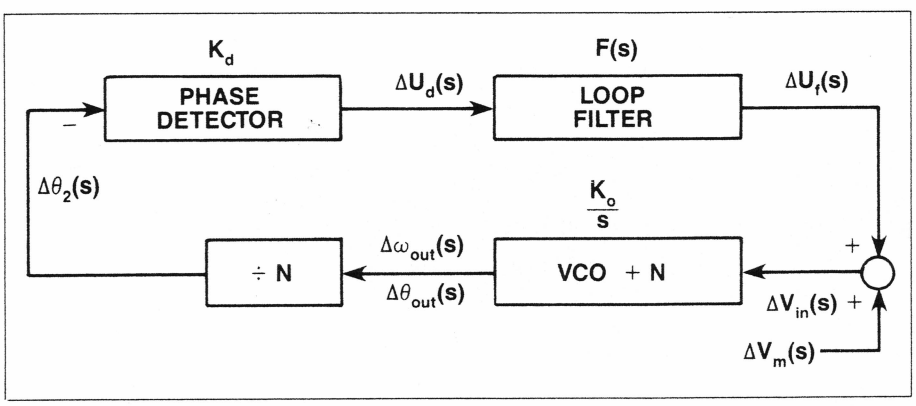

Figure 5. The FM PLL small signal model.

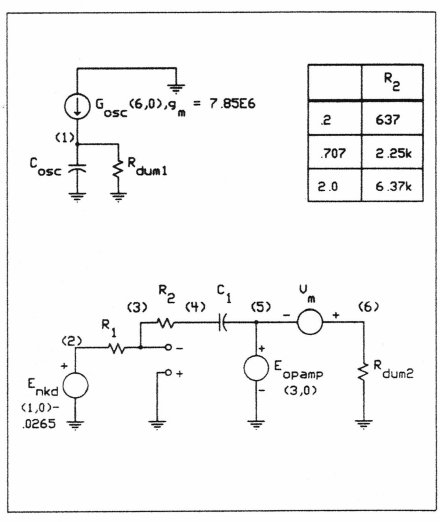

Figure 6. PLL SPICE Model.

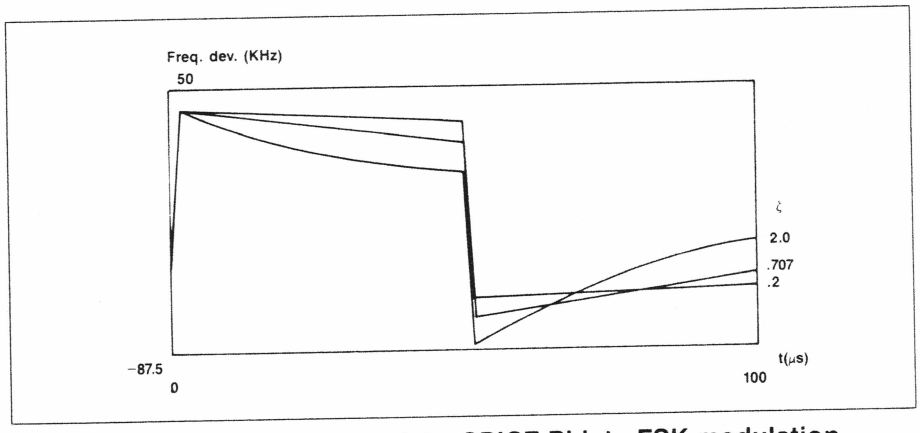

Figure 7. Transient response of the SPICE PLL to FSK modulation.

phase error in pulse width form, so there is undesired energy present at the reference and its harmonics. Some of it gets through the filter to the VCO input, where it causes sidebands. If a noise voltage has frequency ω_m and peak value V_t, then narrow band FM theory (5) shows the sideband to carrier ratio at offset ω to be given by equation 23. Note that this is a magnitude ratio when converting to dB(20 log), and that K_o is in rad/sec/volt.

$$\frac{\text{sideband}}{\text{carrier}}(\omega_m) = \frac{V_t K_o}{2\omega_m} \qquad (23)$$

A PLL using the type 3 loop filter will drive the PD pulse width to approach zero, thus forcing the sideband generating harmonics in the PD output to also approach zero. However, modulation imposed on the PLL will widen the pulse width proportionately, making the sideband problem much worse.

For modulation rates much less than the reference frequency the pulse width may be considered to be a continuous variable. The ratio of the PD pulse width rho to the reference period is:

$$\frac{\varrho}{t_{ref}} = \frac{K_o}{2\pi N}\int_o^t v_m(t)dt \qquad (24)$$

A complex form Fourier series expansion of equation 24, some simplifying approximations, and substitution into equation 23 will show the sideband to the carrier from the nth PD harmonic to be:

(25)

$$\frac{\text{sideband}}{\text{carrier}}(n, t) = \frac{K_o^2 V_{cc}|F(n\omega_{ref})|}{Nn\omega_{ref}}\int_o^t v_m(t)dt$$

Equation 25 is accurate for the first few harmonics, and sets a worst case for higher ones. Determining a worst case for the integral under a specific modulation allows a quick calculation of the worst case sideband to carrier.

If the sideband to carrier is unacceptable, the designer has the option of using a linear PD. The linear PD does not suffer an increase in harmonic content under modulation, but it lacks the wide capture range needed for a wideband synthesizer. Still, it might be the best choice for some applications.

Recently there has been some work done in the area of digital phase detection with reference frequency suppression (6). This type of phase detector would be especially valuable for the FM PLL. Hopefully, these techniques will be incorporated in the future by the major PLL component suppliers.

Conclusion

The FM PLL is a convenient means of obtaining an accurate frequency modulated frequency source. The extension of the normalized form to these sources greatly simplifies their analysis and design. A newly defined parameter, the signal to distortion ratio, is very useful in understanding and minimizing loop distortion.

The integrator error correction method yields a large improvement in distortion, but has a few problems to watch for. Chief among these is the degradation in sideband to carrier ratio, particularly with standard digital phase detection. The methods discussed will allow accurate prediction of performance prior to actual prototyping, thus allowing a decision to be made about the suitability of the FM PLL for a particular application.

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References

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About the Author

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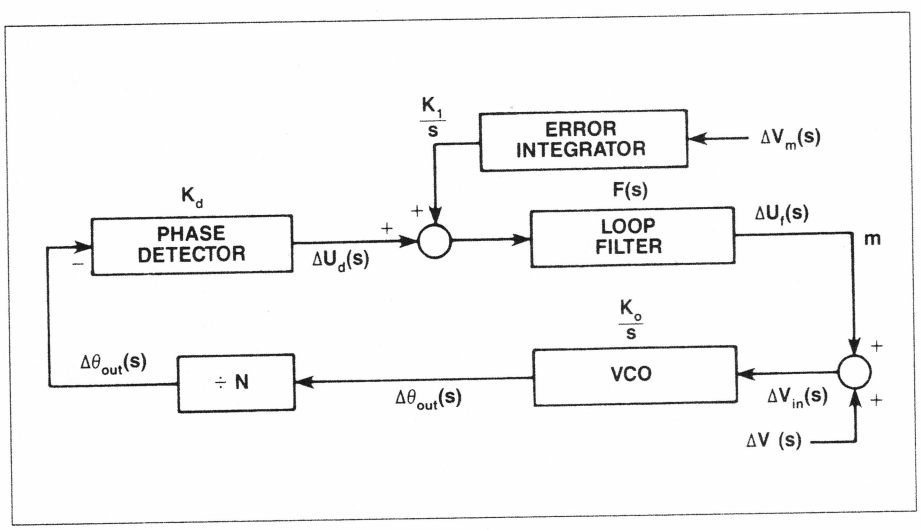

Figure 8. The FM PLL with integrator error correction.