Noise Sources in Ultra-Low Noise Synthesizer Design

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Introduction

Phase noise is an interference source and a dynamic range limit in communications systems. The noise can cause interference both "in-channel" for systems with modulation terms close to the carrier, or further from the channel being used in what's often referred to as adjacent or alternate channel performance. As communications systems are often expected to operate under large link loss conditions, often exceeding 130dB and sometimes exceeding 150dB, it is necessary for them to have a low noise floor, sometimes at the limit of the physically possible. Deliberately designing for this particular kind of noise control is not often taught in electrical engineering curricula, even at the graduate level. Also, in recent years there has been large change in the technology of synthesizer design, with noise control becoming more based on in-loop bandwidth suppression of VCO noise, allowing noisier on-die VCO's to still deliver excellent performance. This noise suppression is particularly important with the high loop bandwidths enabled by modern sigma delta synthesizer IC's using the latest high frequency, low noise crystal reference oscillators.

This is the second article in our low-noise synthesizer design series, and is the moderately longer on-line version. A still more complete version will be posted on the Publications page at www.longwingtech.com. The first article (Ref. 1) covered basic design for functionality and stability. This second article, as well as the upcoming Part 3, will extend the basic methods to specifically cover designing for minimum phase noise. Here, Part 2 focuses on noise sources outside the synthesizer integrated circuit (IC), such as the voltage-controlled oscillator (VCO) and the various loop-filter forms.

The synthesizer IC noise and loop functions for shaping and combining all of the sources will be presented in the next article, revealing how modern synthesizer ICs with on-die VCOs can deliver performance that's often competitive and sometimes superior to synthesizers with low-noise discrete VCOs. The fourth article in this series will cover parts and CAD tools available to the low-noise synthesizer designer, including the latest synthesizer IC's, crystal references, op-amps, and VCO's that enable the very lowest noise designs. The fifth and final article will bring this material together in the form of low-noise synthesizer examples.

Frequency Domain Definition of Phase Noise

We may think of phase noise as the frequency domain spectral density noise surrounding the carrier of a frequency source such as a voltage controlled oscillator (VCO). Phase noise is mostly in the form of phase variation in a compressed oscillator, which will consist of the oscillator's own noise as well as terms from the control and power supply of the oscillator. It is usually described in units of decibels relative to carrier power per Hz, at an offset "f" from the carrier frequency. It is typically divided into regions with well defined slopes, as shown in **Error! Reference source not found.**. Refer to a source such as Ref 1 (Rohde) for a more detailed definition.

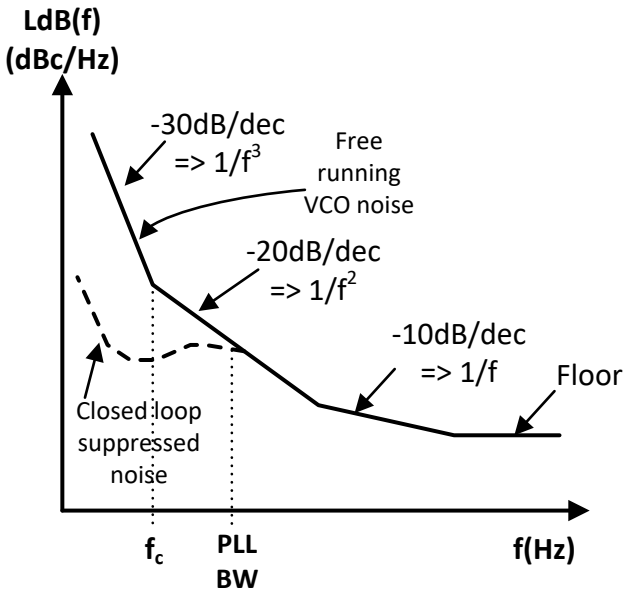

Figure 1: Here the phase noise of a free-running VCO is compared the same VCO when phase-locked, showing the noise suppression within the loop bandwidth. In this article, the dB value of phase noise will be referred to as LdB(f) = 10log(L(f)).

In the above figure, the -30dB/decade part of the free running slope below frequency f_c is flicker noise dominated, which is predominantly caused by baseband flicker noise in the amplifier mixing up around the carrier. The -20dB/decade slope is a basic indicator of Q in the oscillator loop. The -10dB/decade part of the slope is typically only be seen in very high Q oscillators. The floor is generated by the thermal noise raised by the gain and noise figure of the active device. In the locked state the phase noise above the loop bandwidth converges towards the free running noise. Below the loop bandwidth the noise is suppressed by feedback that strives to keep the phase noise equal to the multiplied phase noise of the reference source, which is usually lower than free running as the reference is a very high Q crystal oscillator.

The phase noise as shown in **Error! Reference source not found.** is single sided. Consideration of total noise on both sides, the "spectral density of phase fluctuation" needed to covert phase noise to timing jitter, is discussed in the long version. This distinction will also be important when modeling PLL phase noise in SPICE, a subject presented in the long version of article 3.

Induced Noise in the VCO

Basic Induced Noise: Noise on the input (steering) voltage of the VCO will induce a sideband to carrier spectral component according to:

Equation 1: $$\frac{S}{C} = S_c = \frac{V_n K_{Hz}}{\sqrt{2}\, f}$$

We shall refer to this important relationship as the **"VCO Noise Modulation Function".** This equation is derived by small signal FM theory and a form of it is given in most introductory

communications theory text books. Here K_{Hz} is the same Hz/V steering function of the VCO used in article 1. In the derivation V_n is the rms value of a sinusoidal term. However, if V_n is a spectral noise density, then this sideband to carrier becomes a phase noise density. Since this expression was derived using voltage ratios, converting it to phase noise in dBc is done using *20log*. In synthesizer design this expression is of critical importance because the loop and loop filter do place noise at the VCO steering input that is translated to phase noise output. Naturally it is desired for this induced phase noise to be below the free running noise of the VCO that is approximated by Leeson's Equation (see below).

The noise modulation function may also be used to find the phase noise term due to noise on the supply. The VCO frequency is typically a secondary but important function of supply voltage with a "steering" gain K_{pHz} that is generally about one order of magnitude less than K_{Hz}. Noise is modulated from this source to phase noise by:

Equation 2: $$\frac{S}{C}(\boldsymbol{power\ supply}) = \boldsymbol{S_{cp}} = \frac{\boldsymbol{V_{np}K_{pHz}}}{\sqrt{2}\,\boldsymbol{f}}$$

We see that for both input and power supply noise that a frequency flat noise spectral density will cause phase noise to decline at 20 dB/decade as frequency increases. Over this range of frequency, a constant (over frequency) allowed noise density on steering and power nodes may be specified that keeps induced noise below the VCO free running phase noise on the most important 20dB/dec part of the phase noise curve. The VCO input noise V_{n1} will include PLL loop filter noise. With switching regulators, the suppression required to reduce the power supply noise V_{np} to negligible can exceed **100 dB**. Such high noise suppression will generally require at least one active linear regulator stage plus passive filtering, and may require two active stages. The low noise required of supplies in low noise synthesizers is an often overlooked factor (Part 4).

Loop BW and VCO K_{Hz} Effects on Phase Noise

The physical existence of the induced noise leads us to beware of noise on the VCO input and supply, and to look for effects such noise causes as a function of design choices such as loop BW and VCO gain. Well inside the loop bandwidth such noises are suppressed by PLL closed loop action (covered in Part 3), but at the loop BW and for as much as a decade past it (before higher filter poles take effect) we will have such noise sources inducing extra VCO noise. If this noise is approaching or above the VCO free running noise, then it is only when the first pole takes effect and has had enough frequency skirt to filter down such noise to be negligible that the closed loop noise will match the VCO free running noise.

We know that the minimum noise we will have driving the VCO input will be given by the thermal noise of the zero resistor R_2. From article 1 we have this approximation for R_2:

Equation 3: $$\boldsymbol{R_2} = \frac{\boldsymbol{4\pi N\omega_n\zeta}}{\boldsymbol{K_oI_{pd}}} = \frac{\boldsymbol{2N\omega_n\zeta}}{\boldsymbol{K_{Hz}I_{pd}}} \cong \frac{\boldsymbol{N\omega_L}}{\boldsymbol{K_{Hz}I_{pd}}}$$

For the resistor thermal noise voltage we have the standard equation (Ref. 3, pp. 8-10):

Equation 4: $$\boldsymbol{V_{nR2}} = \sqrt{\boldsymbol{4kTR_2}}$$

In the above k is Boltzman's constant (1.38E-23) and T is absolute temperature (290 at room temp). Putting these two equations together with the induced noise relation Equation 1, we find the minimum induced phase noise at the loop bandwidth f_L to be:

Equation 5: $$L_{MinInduced}(f_L) = \frac{4\pi kTN}{I_{pd}} \frac{K_{Hz}}{f_L}$$

In the locked loop the noise at the loop bandwidth is a critical figure of merit, and with a low noise VCO the induced noise of R_2 is usually an important component of that noise. This induced noise represents a minimum possible noise—even if there were no other PLL noise sources and the VCO were noise free this noise would still exist as the cost of locking the VCO. Additionally, this equation shows that for any given f_L, this important noise component at this critical loop bandwidth frequency is proportional to K_{Hz}. This explains why higher voltage VCO's with lower K_{Hz} are theoretically capable of lower noise, and despite recent advances in integrated performance remain an optimum solution in some applications.

Leeson's Equation for VCO Noise, and its Consequences

The Expanded Leeson Equation: A detailed expression for VCO phase noise is given below, which is an expansion of the famous equation first developed by Leeson (Refs. 2 and 5) and further developed by numerous authors. This expression is a linear power ratio, so in converting it to dB we use 10log. The equation is good to about +/-2dB. We will use the variable "L(f)" for linear carrier to noise power ratio at offset "f", and "L_{dB}(f)" for the decibel variant. In this expression f is offset frequency, f_o is carrier frequency, f_c is the flicker noise corner, k is Boltzman's constant, Q is *loaded* resonator Q, G is loop gain in compression (the reciprocal of VCO loop loss given by $1 - Q_L/Q_0$), F is noise factor in compression, K_{Hz} is VCO gain in Hz/volt, K_{pHz} is VCO power supply pulling in Hz per volt, V_{n1} is spectral noise density at f on the steering input, V_{n2} (also called V_{np} at other points in this article) is spectral noise density at f on the power supply, and P_0 is the power dissipated within the loop (losses from all sources). More detailed information is provided in the full version at www.longwingtech.com.

Equation 6:

$$L(f) \cong \frac{\left(\frac{f_o}{2Q}\right)^2 \frac{GFkT}{2P_0} f_c}{f^3} + \frac{\left(\frac{f_o}{2Q}\right)^2 \frac{GFkT}{2P_0} + \left(\frac{V_{n1}(f)K_{Hz}}{\sqrt{2}}\right)^2 + \left(\frac{V_{n2}(f)K_{pHz}}{\sqrt{2}}\right)^2}{f^2} + \frac{\frac{GFkT}{2P_0} f_c}{f} + \frac{GFkT}{2P_0}$$

Referring VCO Noise to Input: The Leeson Equation and the earlier relationship on induced noise show that VCO noise at any frequency can be referred to the VCO input as a noise voltage that generates that same VCO noise on the output of a noiseless VCO. Given L(f) or LdB(f) we may write for input referred VCO noise V_{nvco}:

Equation 7: $$V_{nvco} = \frac{\sqrt{2}\, f 10^{\frac{LdB(f)}{20}}}{K_{Hz}} = \frac{\sqrt{2}\, f \sqrt{L(f)}}{K_{Hz}}$$

Noise on the power supply also generates noise on VCO output, which will often require ultra-low noise supplies for the VCO (Part 4). It will be useful in calculations and modeling to also refer the sideband to carrier effect of noise on the supply to the VCO input, where it can be rms summed with the other noises on that critical node, and then processed by the loop. Supply noise density is referred to the VCO input according to:

Equation 8: $$V_{npin} = V_{np} \frac{K_{pHz}}{K_{Hz}}$$

In this equation, K_{pHz} is the VCO gain with respect to the power supply input in Hz/V, V_{np} is the spectral voltage noise density the supply, and V_{npin} is the supply noise referred to the steering input of the VCO.

Advantage of Higher Frequency: Digitally programmable dividers are almost always available on modern synthesizers to allow output at lower frequencies. If an octave of higher frequency coverage is available from a set of on-die VCO's, then effectively any lower frequency can be delivered by the dividers. The resulting very wide frequency range available (often tens of MHz to many GHz) is one of the main advantages of integrated VCO's as compared to discrete VCO's. While a small fraction of discrete VCO's are capable of an octave of tune range that can emulate this behavior, generally only those octave VCO's with the best performance and with maximum frequency below about 4 GHz have better phase noise than integrated VCO's (see Part 4 for examples).

When a frequency source is divided by a factor N, phase noise at the divider output will generally go down 20logN as compared to the input, down to a divider noise floor. For example, when frequency is divided by 2, phase noise goes down 6dB.

In practice for integrated VCOs total resonator Q tends to rise for lower frequencies as frequency increases (driven by increasing inductor Q), reaches a peak, and then declines as frequency continues to increase. Referring to Leeson's Equation above, if at lower frequency total Q is approximately linearly proportional to frequency, then if frequency doubles phase noise is flat with increasing frequency. In that case dividing down by 2 improves phase noise by 6 dB compared to a VCO running at the lower frequency with half the Q. This is used to advantage in fully integrated synthesizer design, where there often exists an optimum VCO frequency for minimum *normalized* phase noise. Normalized phase noise refers to the quality of the phase noise as a figure of merit independent of RF frequency, and it is minimum when Q is maximum. Dividing down from this optimum frequency then yields significantly better phase noise than a VCO at the lower frequency could directly achieve.

If Q is effectively flat with frequency, the phase noise at a test offset frequency typically goes up approximately 6 dB for every doubling of the frequency. Since phase noise is reduced 6 dB by every digital divide by 2, dividing the 2X higher VCO frequency by 2 will effectively give the same phase noise as the original lower frequency. In this zone there is little or no phase noise advantage to the higher frequency, but the advantage of having a higher frequency available for when it is needed is present.

If the Q is going down with frequency, as it often is for the highest frequency on-die VCO's, then normalized phase noise is going up as frequency increases. In this case the phase noise performance of a lower frequency VCO cannot be fully recovered by dividing down. This is a factor to be aware of when choosing a synthesizer chip. Sometimes a lower frequency (and usually lower cost) device is lower noise than a higher frequency device whose output is divided down.

High Voltage, Low K_{Hz} VCO Noise Improvement*:* When better far out noise is needed than a fully integrated VCO synthesizer can provide (Part 5), the usual method is a discrete higher voltage VCO with low K_{Hz}. A discrete VCO allows higher Q than integrated, and Leeson's Equation shows noise is inversely proportional to Q^2, so this is a very strong effect. A higher voltage VCO allows greater voltage swings and higher power also, and Leeson's shows phase noise being inversely proportional to power. A third significant effect favoring the discrete higher tune range VCO is that covering a given tune range allows lower $K_{Hz,}$ and as shown above induced phase noise power is directly proportional to K_{Hz}. These factors can allow an extremely low noise discrete VCO to sometimes offer a superior noise solution at medium offsets, and quite often at far out offsets.

Converting Phase Noise to Time Jitter: See the full length version at www.longwingtech for these relations**.**

Passive Part Noises: See the full length version for descriptions and equations of noises other than thermal. These include excess resistor (current) noise, and the noises of ceramic, tantalum, and film capacitors.

Filter Noises and Limits

Noise in the loop filter is usually strongly suppressed well inside the loop bandwidth, as will be presented in Part 3 and demonstrated in the examples of Part 5. But, around the loop bandwidth and for up to a decade or so past the loop bandwidth, the noise of the filter may dominate the phase noise. It was shown earlier how the minimum induced noise is given by R_2 thermal noise, and that his noise power is proportional to the product of loop bandwidth f_L and VCO gain K_{Hz}. As loop bandwidth is directly proportional to R_2 and other resistors in the passive loop filter generally scale with R_2, the filter noise may set limits on the bandwidth to be used in the PLL. The active loop filter has the advantage that the largest resistor noise will generally be from R_2, but the disadvantage of op amp and reference noises. In the active filter case, the noise current of the op amp also flows through R_2, and this can be an even worse noise source than the thermal noise of R_2.

Second Order Passive Filter Noise: The 2^{nd} order passive filter has the form shown in Figure 2.

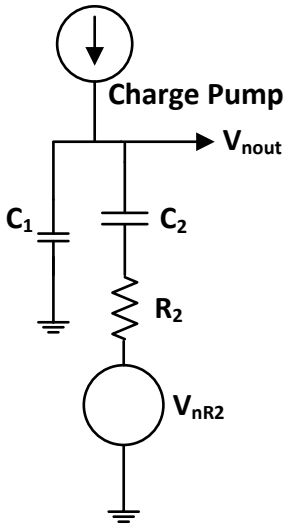

Figure 2: Shown here is the second-order loop filter with its single noise source, the thermal noise in R_2.

Analysis of the above circuit yields:

Equation 9: $$|V_{noutR2}|^2 = \frac{4kTR_2}{\left(1+\frac{C_1}{C_2}\right)^2+(2\pi f R_2 C_1)^2}$$

The filter impedance Z_f as seen by the charge pump is:

Equation 10: $$Z_f = \frac{sC_2R_2+1}{s(sC_1C_2R_2+C_1+C_2)}$$

If the noise of the charge pump and dividers is modeled as a noise current I_{pn}, then:

Equation 11: $$|V_{ncp}|^2 = I_{pn}^2 |Z_f|^2 = I_{pn}^2 \frac{\omega^2 C_2^2 R_2^2 + 1}{\omega^4 R_2^2 C_1^2 C_2^2+\omega^2(C_1+C_2)^2}$$

The total filter noise voltage squared is then the sum of these two noise powers. This form of loop filter is the lowest possible noise, as it only has R_2 as an internal noise source. This equation may be reused for the R_2 noise term in the slow slew active loop filter also.

Third Order Passive Filter Noise: The 3rd order passive loop filter is shown in Figure 3. In analyzing for V_{nout} we define several intermediate impedances. For example, $Z_{3\text{-}1}$ is the impedance of C_1 in parallel with the series impedance of R_3 and C_3. $Z_{2\text{-}1}$ is the impedance of C_1 in parallel with the series impedance of R_2 and C_2. We then apply voltage and current division to the different blocks.

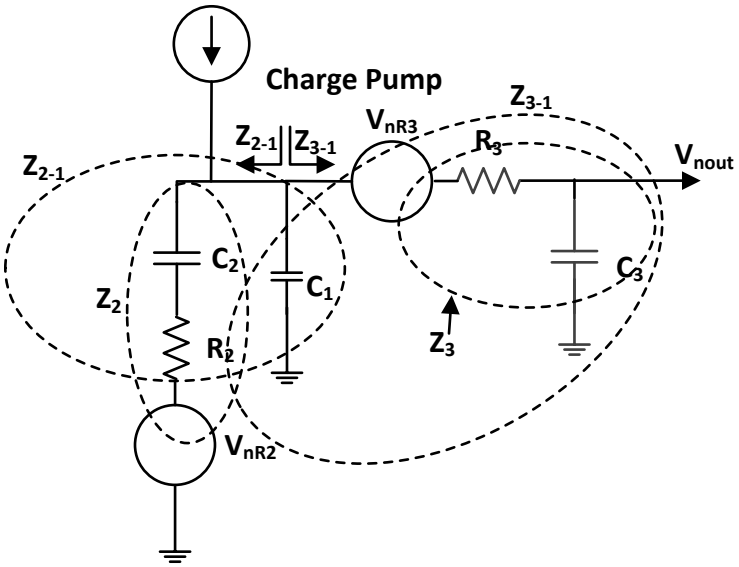

Figure 3: Depicted here is the third-order passive loop filter with intermediate impedances defined for finding V_{nout}, and its two thermal noise sources.

Going through this process, we find the below set of equations.

Equation 12: $$\boldsymbol{Z_f(s) = \frac{1+sT_2}{s\,A_0(1+sT_1)(1+sT_3)} = \frac{1+sC_2R_2}{s\left(A_2\,s^2+A_1\,s+A_0\right)}}$$

Equation 13: $$\boldsymbol{T_2 = R_2C_2}$$

Equation 14: $$\boldsymbol{T_3 = R_3C_3}$$

Equation 15: $$\boldsymbol{T_{3-1} = \frac{C_1C_3}{C_1+C_3}\,R_3}$$

The noise from R_2 at the output is:

Equation 16: $$\boldsymbol{V_{nout2} = \frac{4kTR_2}{\frac{C_1+C_3}{C_2}(sT_2+1)(sT_{3-1}+1)+(sT_3+1)}}$$

The noise from R_3 at the output is:

Equation 17: $$\boldsymbol{V_{nout3} = \frac{4kTR_3\,[C_1(sT_2+1)+C_2]}{(sT_3+1)[C_1(sT_2+1)+C_2]+C_3(sT_2+1)}}$$

And then finally,

Equation 18: $$V_{nout} = \sqrt{V_{nout2}^2 + V_{nout3}^2}$$

Both R_2 and thus R_3 are smaller with the lower N value of modern fractional N synthesizers with high phase detector frequencies (see second order normalized form approximation of R_2), as compared to older integer N designs, and thus have lower noise. Oftentimes R_3 is in the range of about R_2 to 3X R_2. We may thus approximate the noise voltage to expect from the properly designed 3rd order passive loop filter to be about 1.5 to 2X that of the 2nd order filter. This lower R_2 and R_3 value, along with higher frequency to be divided down to the application frequency, and the higher phase detector frequency and loop bandwidth of the modern sigma delta PLL as will be presented in Part 3, are all essential factors in lower total noise.

Third Order Buffered Semi-Active Filter: A common active filter strategy is to break the 3rd or 4th order passive filter up with an op amp buffer in the middle that drives the final one or two RC stages, which shall be referred to here as "semi-active". This can be beneficial if the noise of R_3 and R_4 is noticeable (since smaller resistor values may be used in the active case), if moderately greater tune voltage is needed, or if VCO input leakage current is on the high side side of typical. Since it is not the most recommended active filter form, the analysis and design of this filter form is deferred to the full version of this article posted on the Longwing website.

Fourth Order Active Filter Noise: The design methodology for the "slow slew mode" 4th order active filter was given in the first article of this series. This active filter architecture is designed to reduce the bandwidth and slew rate requirements on the op amp, at which it is partially successful. The use of the inverting mode with R_2 and C_2 in the feedback path allows this form to provide higher tune voltages with low noise gain. Current flows through R_3 and then through R_2-C_2 to charge up the op amp output to whatever voltage is needed. The input RC is intended to shield the op amp from the high slew rate and bandwidth of the charge pump output.

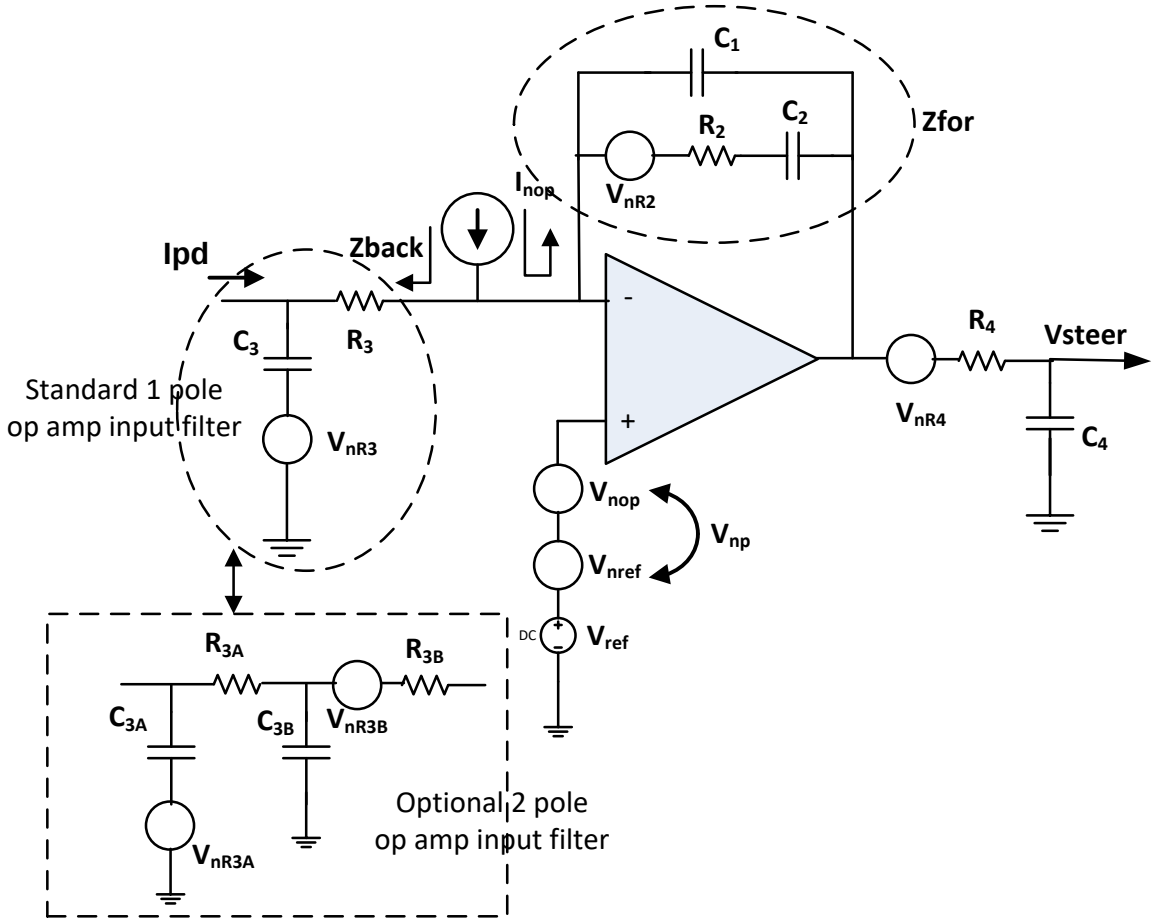

Figure 4: The 4th order active loop filter with the option to become 5th order. The noise sources to be analyzed are shown.

However, despite its benefits in limiting the op amp's exposure to high frequency signals from the charge pump, it may be advantageous to add an additional input RC stage. As pointed out by Banerjee, experimental evidence (Ref. 4, 5th ed., pp.371-372) indicates that the op amp in an active loop filter not being fast enough sometimes seems to cause a several dB rise in the 1/f noise of the PLL, presumably due to pulse widening allowing through more charge pump 1/f noise.

The noise on steering output of the active filter may be characterized as the sum of the noise powers from the plus input, from the minus input, from the forward impedance, and in the final RC stage.

The minus input internal filter noise is the thermal noise of R_3, gained up by:

Equation 19: $$V_{nopR3}^2 = 4kTR_3 \left|\frac{Z_{for}}{Z_{back}}\right|^2$$

We can generate this noise over frequency using the next several relationships.

Equation 20: $$Z_{back} = R_3 + \frac{1}{sC_3R_3} = \frac{sC_3R_3+1}{sC_3}$$

Equation 21: $$Z_{for} = \frac{1+sR_2C_2}{s(C_1+C_2+sR_2C_2C_1)}$$

Next, we consider the gained noise from the plus input of the op amp. This is the rms sum V_{np} of the reference noise and the op amp's own noise, appropriately gained, given by:

Equation 22: $$V_{nopp}^2 = V_{np}^2 \left|1 + \frac{Z_{for}}{Z_{back}}\right|^2$$

The below magnitude squared functions are convenient to use.

Equation 23: $$|Z_{back}|^2 = R_3^2 + \frac{1}{\omega^2 C_3^2} = \frac{\omega^2 R_3^2 C_3^2 + 1}{\omega^2 C_3^2}$$

Equation 24: $$\left|Z_{for}\right|^2 = \frac{\omega^2 C_2^2 R_2^2 + 1}{\omega^4 R_2^2 C_1^2 C_2^2 + \omega^2 (C_1+C_2)^2}$$

The noise generated by R_2 is found taking into account that the minus input of the op amp is a "virtual ground". Op amp feedback holds it equal to the plus input, so noise from R_2 comes straight through to the output, except for being filtered within Z_{for} when $C_1 > 0$.

Equation 25: $$\left|V_{nopR2}\right|^2 = \frac{4kTR_2}{\left(1+\frac{C_1}{C_2}\right)^2 + (2\pi f R_2 C_1)^2}$$

The noise generated on the op amp output by the op amp noise current is again found by noting that the minus input is kept equal to the plus input by op amp feedback. The only way for that to hold is for I_{nop} to flow totally through Z_{for} and not through Z_{back}.

Equation 26: $$\left|V_{nopInop}\right|^2 = I_{nop}^2 \left|Z_{for}\right|^2$$

For the sake of convenience, we may count the noise of R_4 as part of op amp output. We now have all the noise terms at the op amp output.

Equation 27: $$V_{noptot}^2 = V_{nopR3}^2 + V_{nopp}^2 + V_{nopR2}^2 + V_{nopInop}^2 + V_{nR4}^2$$

This noise needs merely to be passed through a now noiseless R_4-C_4 filter to give the noise from the active filter to be presented to the steering input of the VCO.

Equation 28: $$V_{nout}^2 = \frac{V_{noptot}^2}{\omega^2 C_4^2 R_4^2 + 1}$$

With the above we have all the major open loop noises to be shaped by the loop except for what is sometimes called the "PLL noise". This is something of a misleading term, since it typically means just the noise of the charge pump and dividers in the synthesizer IC, not the total PLL noise. It is not given above in the noise sources review as it is normally specified as a closed loop noise after shaping. It will be covered in the next article along with the methods for analyzing how noise is shaped, optimum loop bandwidth, and the synthesizer IC figure of merit for evaluating chip noise.

About the Author: Farron Dacus is an RF design consultant in Dallas, Texas. His BSEE and MSEE are from the University of Texas, and he has over 30 years of experience ranging from IC's to circuits to systems in low noise RF, short range radio / IoT, cellular, military communications, and aircraft radios. He may be reached at farron.dacus@longwingtech.com.

Article 2 References

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5. "*Fundamentals of RF Circuit Design with Low Noise Oscillators*", Jeremy Everard, John Wiley and Sons, 2001. This reference is particularly excellent for its detailed examination of Leeson's Equation, with variations for how impedance is defined and used within the oscillator loop.