Noise Sources in Ultra-Low Noise Synthesizer Design

Farron L. Dacus, RF Design Consultant
Longwing Technology
www.longwingtech.com

Introduction

This is the second article in our low noise synthesizer design series. This is the full length version containing some information not shown the print and digital versions published in "Microwaves & RF" in their February 2019 issue. The first article (Dec. 2018) covered basic design for functionality and stability. This second article as well as the third will extend the basic methods to specifically cover designing for minimum phase noise. This article will cover the noise sources outside the synthesizer IC. The synthesizer IC noise and loop functions for combining all the sources will be shown in the next article. The 4th article in this series will cover parts and CAD tools available to the low noise synthesizer designer. The 5th and final article will bring this material together in the form of low noise synthesizer examples.

Phase noise is an interference source and a dynamic range limit in communications systems. The various noise terms contributing to phase noise outside of the synthesizer IC will be quantified here, specifically the VCO, crystal reference, power supply noise effect, the noise of the various filter forms, and the various noises of resistors and capacitors. Additional material includes phase noise represented as time jitter, additional forms of noise beyond thermal for passive parts, graphs of key transfer functions, and details of the semi-active/buffered form of active loop filter.

Phase noise can cause interference both "in-channel" for systems with modulation terms close to the carrier, or farther from the channel in use in what is often referred to as adjacent or alternate channel performance. Radar and RFID are systems where a low-level reflected signal close to the carrier must be received in the presence of a strong carrier, and thus are quite sensitive to in-channel phase noise. Microwave and satellite communications using high bit per symbol modulation methods are also examples of systems where in-channel phase noise can be a limiting factor. Examples of systems needing particularly low farther out noise include cellular base stations (which typically require better adjacent channel noise performance than handsets), land mobile radio and related military communications systems where a narrow channel contributes to adjacent channel interference being relatively close to the carrier, and aircraft radio where multiple transceivers operate in close proximity and where transmitted phase noise even relatively far from the carrier can still cause direct interference. Amateur radio is an application where nearby strong transmissions in space and frequency are generally not coordinated within a system, resulting in phase noise as an interfering source that can be both close in or farther out. As a final major example, test equipment must have noise significantly below the device under test to get accurate measurements, and the finest possible phase noise both close in and farther out is generally desired. Phase noise requirements for some of these applications will be derived in the long version of article 3. The way in which modern sigma delta, fractional N, high bandwidth synthesizers with on-die VCO's can so strongly suppress phase noise as to be competitive and sometimes superior to low noise discrete VCO synthesizers will be covered in article 3, with examples in article 5.

Frequency Domain Definition of Phase Noise

Frequency sources are never perfect, being corrupted by frequency error, harmonic content, and noise. The noise is mostly in the form of phase variation in a compressed oscillator, where the compression limits amplitude noise. We thus speak of the frequency domain spectral density noise surrounding the carrier of a frequency source such as a voltage controlled oscillator (VCO) as being phase noise. It is usually described in units of decibels relative to carrier power per Hz, at an offset "f" from the carrier frequency. It is typically divided into regions with well defined slopes, as shown in Figure 1. Refer to a source such as Ref 1 (Rohde) for a more detailed definition.

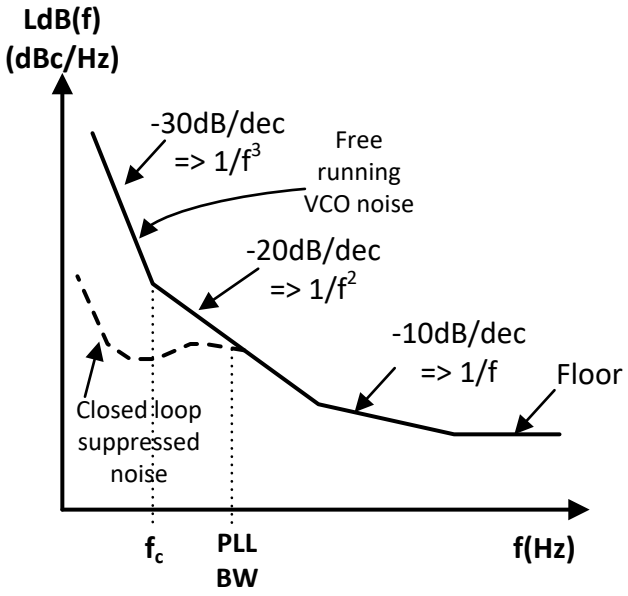

Figure 1: Here the phase noise of a free-running VCO is compared the same VCO when phase-locked, showing the noise suppression within the loop bandwidth. In this article, the dB value of phase noise will be referred to as LdB(f) = 10log(L(f)).

In the above figure, the -30dB/decade part of the slope below frequency fc is flicker noise, which is predominantly caused by baseband flicker noise in the amplifier mixing up around the carrier. The -20dB/decade slope is a basic indicator of Q in the oscillator loop. Deriving the characteristics of this part of the slope is a key element in VCO analysis and design. The -10dB/decade part of the slope is flicker noise that may be exposed by the -20dB/decade part of the slope dropping into negligibility, though this will typically only be seen in very high Q oscillators. The floor is generated by the thermal noise raised by the gain and noise figure of the active device. Since phase noise is a relative measure (relative to carrier power), a high power oscillator can have a relative floor separated from carrier power by an amount greater than the absolute thermal floor of -174dBm/Hz. In the locked state the phase noise above the loop bandwidth converges towards the free running noise. Below the loop bandwidth the noise is suppressed by feedback that strives to keep the phase noise equal to the multiplied phase noise of the reference source, which is usually lower than free running as the reference is a very high Q crystal oscillator.

The phase noise as shown in Figure 1 is single sided, one side of what would be displayed on a spectrum analyzer. When we consider the total noise in both sidebands (such as

is necessary when finding timing jitter), then this is referred to as the "spectral density of phase fluctuation", given by (Ref. 1, p. 81):

Equation 1: $S_\theta = 2L(f)$

Induced Noise in the VCO

Basic Induced Noise: Noise on the input (steering) voltage of the VCO will induce a sideband to carrier spectral component according to:

Equation 2: $\frac{S}{C} = S_c = \frac{V_n K_{Hz}}{\sqrt{2}\, f}$

We shall refer to this important relationship as the **"VCO Noise Modulation Function".** This equation is derived by small signal FM theory and is given in most introductory communications theory text books. Here K_{Hz} is the same Hz/V steering function of the VCO used in the loop design methodology of article 1. In the derivation V_n is the rms value of a sinusoidal term. However, the analysis is not limited to discrete modulation terms. If V_n is a spectral noise density, then this sideband to carrier becomes a phase noise density. Since this expression was derived using voltage ratios, converting it to phase noise in dBc is done using *20log*.

In synthesizer design this expression is of critical importance because the loop and loop filter do place noise at the VCO steering input that is translated to phase noise output. Naturally it is desired for this induced phase noise to be below the free running noise of the VCO that is approximated by Leeson's Equation (see below). If this term is 6dB below the free running noise, it will degrade the free running VCO noise by about 1dB. Note that if modulating noise V_n is flat (such as resistor thermal noise), then the induced noise is at -20dB/decade.

It was discussed in article 1 how the VCO in a control systems sense acts as an integrator of input voltage to output phase. The output phase noise of the VCO (and the crystal oscillator also if it has a tune input) in radians rms with respect to a noise density input V_{nsteer} is given by the magnitude of the integration function:

Equation 3: $|\theta_n(\omega)| = \frac{V_{nsteer}(\omega) K_o}{\omega}$

We may change the frequency variable from "ω" to "f" since we are *by definition* considering noise on a per Hz basis, and thus $V_{nsteer}(\omega) = V_{nsteer}(f)$ on a per Hz basis at a particular frequency, whether that frequency is given in rad/s or Hz. We also note that $K_o/\omega = K_{Hz}/f$. Thus, in the closed loop case with $V_{nsteer} = V_{nsteercl}$:

Equation 4: $|\theta_n(f)| = |\theta_n(\omega)| = \frac{V_{nsteercl}(\omega) K_o}{\omega} = \frac{V_{nsteercl}(f) K_{Hz}}{f}$

This differs from the noise sideband to carrier ratio only by the square root of 2 in the denominator of Equation 2. Thus:

Equation 5: $\frac{S_n}{C}(f) = \frac{|\theta_n|}{\sqrt{2}}$

We then have:

Equation 6: $L_n(f) = \left(\frac{S_n}{C}\right)^2 = \frac{|\theta_n(f)|^2}{2} = \frac{S_\theta}{2}$

This result is seen to merely be the consideration of noise power on one side of the carrier vs. both sides. This relationship of induced phased noise is useful when the noises in the block diagram of the PLL are being considered, where the noise "θ_n" in the VCO or crystal reference output is what exists in the loop, but where we often wish to consider the single sided phase noise in the frequency source.

The noise modulation function may also be used to give a phase noise term due to noise on the supply. The VCO frequency is typically a secondary but important function of supply voltage with a "steering" gain K_{pHz} that is generally about one order of magnitude less than K_{Hz}.

Equation 7: $\frac{S}{C}(power\ supply) = S_{cp} = \frac{V_{np}K_{pHz}}{\sqrt{2}\,f}$

We see that for both input and power supply noise that a flat noise spectral density will cause phase noise to decline at 20 dB/decade as frequency increases, which is similar to the natural VCO phase noise shape above the flicker corner and below the floor. Over this range of frequency, a constant (frequency flat) allowed noise density on steering and power nodes may be specified. The VCO input noise V_{n1} will include PLL loop filter noise, of which we will have quite a bit to say in this article. With switching regulators, the suppression required to reduce the power supply noise V_{np} to negligible can exceed **100 dB**. This will often require two levels of linear regulation plus passive filtering. Linear regulators without RC filtering may have a spectral noise density that is typically too high to allow directly on the supply of a low noise VCO. A classic "low noise" regulator typically displays about 20-80 nV per root Hz spectral noise density, whereas for a modern low noise synthesizer we typically need less than 10 nV per root Hz, and may need less than 2nV. Though in recent years lower supply noise has become available in fully integrated form, the very lowest noises may require custom discrete circuitry (Part 4).

With deliberate careful design the spectral noises on the VCO input and power supply can be made negligible or at least only moderately degrading, though if neglected these can easily become dominant noise sources.

Loop BW and VCO K_{Hz} Effects on Phase Noise

The physical existence of the induced phase noise leads us to beware of noise on the VCO input and power supply, and to look for effects such noise causes as a function of design choices such as loop BW and VCO gain. Well inside the loop bandwidth such noises are suppressed by PLL closed loop action, but at the loop BW and for as much as a decade past it we will have such noise sources acting unimpeded in inducing extra VCO noise. If this noise is approaching or above the VCO free running noise, then it is only when the first pole takes effect and has had enough frequency skirt to filter down such noise to be negligible that the closed

loop noise will match the VCO free running noise. We know that the minimum noise we will have driving the VCO input will be given by the thermal noise of the zero resistor R_2, and that other noises such as from additional resistors and possibly an op amp are likely to be present.

From article 1 we have this approximation for R_2:

Equation 8: $$R_2 = \frac{4\pi N \omega_n \zeta}{K_o I_{pd}} = \frac{2N\omega_n\zeta}{K_{Hz} I_{pd}} \cong \frac{N\omega_L}{K_{Hz} I_{pd}}$$

For the resistor thermal noise voltage we have the standard equation (Ref. 5, pp. 8-10):

Equation 9: $$V_{nR2} = \sqrt{4kTR_2}$$

In the above k is Boltzmann's constant (1.38E-23) and T is absolute temperature (290 at room temp). Putting these two equations together with the induced noise relation Equation 2, we find the minimum induced phase noise as:

Equation 10: $$L_{MinInduced}(f_{ref}) = \frac{4\pi kTN}{I_{pd}} \frac{K_{Hz} f_L}{f_{ref}^2}$$

This quantity is in relative power, so 10log is used to convert it to dB phase noise.

This induced noise is most likely to be visible around and just beyond the loop bandwidth, where it is not suppressed by the loop nor yet filtered by higher order loop filter poles. If we let the offset of interest be equal to the loop bandwidth f_L, then:

Equation 11: $$L_{MinInduced}(f_L) = \frac{4\pi kTN}{I_{pd}} \frac{K_{Hz}}{f_L}$$

This simple interpretation is quite revealing as one of the reasons the noise of the integrated VCO synthesizer can be highly competitive. The integrated VCO has a high K_{Hz} and pays a price for that in induced noise, but with a high phase detector frequency thus a smaller divide value N, and a higher f_L, its induced noise in practice is more constrained than might be expected.

In the locked loop the noise at the loop bandwidth is a critical figure of merit, and with a low noise VCO the induced noise of R_2 is usually an important component of that noise. This induced noise represents a minimum possible noise—even if the VCO were noise free this noise would still exist as the cost of locking the VCO. So additionally, this equation shows that for any given f_L, this important noise component at this critical loop bandwidth frequency is proportional to K_{Hz}. This explains why higher voltage VCO's with lower K_{Hz} are theoretically capable of lower noise, and despite recent advances in integrated performance remain an optimum solution in some applications.

Leeson's Equation for VCO Noise, and its Consequences

The Expanded Leeson Equation: A detailed expression for VCO phase noise is given below, which is an expansion of the famous equation first developed by Leeson (Refs. 1, 2, and 3) and further expanded upon by numerous authors. This equation is derived in a linear approximation of the loop gain and phase, where the oscillator loop is "opened" for analysis purposes similarly to how the open loop gain and phase of the PLL are evaluated. This expression is a linear power ratio, so in converting it to dB we use *10log*. We will use the variable "L(f)" for linear carrier to noise power ratio at offset "f", and "$L_{dB}(f)$" for the decibel variant.

There are a variety of such equations presented by different authors, which greatly varying amounts of detail in what conditions are taken into account. For the crucial -20dB/decade part of the slope, a particularly thoughtful and detailed analysis is presented by Everard (Ref. 3, pp.179-196), which takes into account loaded vs unloaded Q, losses in the loop, input and output impedance in the loop, and point used for power extraction. Everard demonstrates that depending on conditions, the ideal loaded Q for best phase noise will be about ½ to 2/3 of unloaded Q. Another way of saying this is that the compressed gain in the oscillator loop is ideally about 6 to 9 dB. Everard reports that in his extensive academic research, the accuracy of the resulting expression is about +/-2dB, which is also in keeping with the author's experience as a low noise VCO designer.

Here we are concerned with having an approximately correct expression taking the main features into account, and showing the main slopes that result in the phase noise curve. In this expression f is offset frequency, f_o is carrier frequency, f_c is the flicker noise corner, k is Boltzman's constant, Q is *loaded* resonator Q, G is loop gain in compression (the reciprocal of VCO loop loss given by $1 - Q_L/Q_0$), F if noise factor in compression, K_{Hz} is VCO gain in Hz/volt, K_{pHz} is VCO power supply pulling in Hz per volt, V_{n1} is spectral noise density at f on the steering input, V_{n2} (also called V_{np} in this article series) is spectral noise density at f on the power supply, and P_0 is the power dissipated within the loop (losses from all sources). If the oscillator is in current compression, P_0 is about 0.5 I^2 Z, where I is the bias current and Z is the total dissipating impedance of all loss sources. For an amplifier driving a lossy resonator, Z is approximately the effective resonator loss resistance taking loaded Q into account.

Equation 12:

$$L(f) \cong \frac{\left(\frac{f_o}{2Q}\right)^2 \frac{GFkT}{2P_0} f_c}{f^3} + \frac{\left(\frac{f_o}{2Q}\right)^2 \frac{GFkT}{2P_0} + \left(\frac{V_{n1}(f)K_{Hz}}{\sqrt{2}}\right)^2 + \left(\frac{V_{n2}(f)K_{pHz}}{\sqrt{2}}\right)^2}{f^2} + \frac{\frac{GFkT}{2P_0} f_c}{f} + \frac{GFkT}{2P_0}$$

In this equation we have the four main slopes shown in Figure 1. The -10dB/dec term (proportional to f^{-1}) is often too low to be detectable in a VCO, but is often visible in an ultra-high Q oscillator like a crystal reference. This expression expands upon Everard's basic presentation by adding terms for flicker noise, noise induced by input (steering) and supply noises, and noise floor. In comparing this equation to Everard's work, it is seen that this is the case where the loop amplifier output impedance is much less than the resonator it drives, and where P_0 is all losses

combined. The case where the amplifier (or loop) output impedance is similar to the input impedance will have this same noise function, except degraded by 3dB.

Referring VCO Noise to Input: The Leeson Equation and the earlier relationship on induced noise show that VCO noise at any frequency can be referred to the VCO input as a noise voltage that generates that same VCO noise on the output of a noiseless VCO. Given L(f) or LdB(f) we may write for input referred VCO noise V_{nvco}:

Equation 13: $$V_{nvco} = \frac{\sqrt{2}\, f 10^{\frac{LdB(f)}{20}}}{K_{Hz}} = \frac{\sqrt{2}\, f \sqrt{L(f)}}{K_{Hz}}$$

As noted above, noise on the power supply also generates noise on VCO output, which will often require ultra-low noise supplies for the VCO (Part 4). It will be useful in calculations and modeling to also refer the sideband to carrier effect of noise on the supply to the VCO input, where it can be rms summed with the other noises on that critical node, and then processed by the loop. Supply noise density is referred to the VCO input according to:

Equation 14: $$V_{npin} = V_{np} \frac{K_{pHz}}{K_{Hz}}$$

In this equation, K_{pHz} is the VCO gain with respect to the power supply input in Hz/V, V_{np} is the spectral voltage noise density the supply, and V_{npin} is the supply noise referred to the steering input of the VCO.

Advantage of Higher Frequency: Digitally programmable dividers are almost always available on modern synthesizers to allow output at lower frequencies. If an octave of higher frequency coverage is available from a set of on-die VCO's, then effectively any lower frequency can be delivered by the dividers. The resulting very wide frequency range available (often tens of MHz to many GHz) is one of the main advantages of integrated VCO's as compared to discrete VCO's. While a small fraction of discrete VCO's are capable of an octave of tune range that can emulate this behavior, generally only those octave VCO's with the best performance and with maximum frequency below about 4 GHz have better phase noise than integrated VCO's (see Part 4 for examples).

When a frequency source is divided by a factor N, phase noise at the divider output will generally go down 20logN as compared to the input, down to a divider noise floor. For example, when frequency is divided by 2, phase noise goes down 6dB.

In practice for integrated VCOs total resonator Q tends to rise for lower frequencies as frequency increases (driven by increasing inductor Q), reaches a peak, and then declines as frequency continues to increase. Referring to Leeson's Equation above, if at lower frequency total Q is approximately linearly proportional to frequency, then if frequency doubles phase noise is flat with increasing frequency. In that case dividing down by 2 improves phase noise by 6 dB compared to a VCO running at the lower frequency with half the Q. This is used to advantage in fully integrated synthesizer design, where there often exists an optimum VCO frequency for minimum *normalized* phase noise. Normalized phase noise refers to the quality of the phase noise as a figure of merit independent of RF frequency, and it is minimum when Q is

maximum. Dividing down from this optimum frequency then yields significantly better phase noise than a VCO at the lower frequency could directly achieve.

If Q is effectively flat with frequency, the phase noise at a test offset frequency typically goes up approximately 6 dB for every doubling of the frequency. Since phase noise is reduced 6 dB by every digital divide by 2, dividing the 2X higher VCO frequency by 2 will effectively give the same phase noise as the original lower frequency. In this zone there is little or no phase noise advantage to the higher frequency, but the advantage of having a higher frequency available for when it is needed is present.

If the Q is going down with frequency, as it often is for the highest frequency on-die VCO's, then normalized phase noise is going up as frequency increases. In this case the phase noise performance of a lower frequency VCO cannot be fully recovered by dividing down. This is a factor to be aware of when choosing a synthesizer chip. Sometimes a lower frequency (and usually lower cost) device is lower noise than a higher frequency device whose output is divided down.

High Voltage, Low K_{Hz} VCO Noise Improvement*:* When better far out noise is needed than a fully integrated VCO synthesizer can provide (Part 5), the usual method is a discrete higher voltage VCO with low K_{Hz}. A discrete VCO allows higher Q than integrated, and Leeson's Equation shows noise is inversely proportional to Q^2, so this is a very strong effect. A higher voltage VCO allows greater voltage swings and higher power also, and Leeson's shows phase noise being inversely proportional to power. A third significant effect favoring the discrete higher tune range VCO is that covering a given tune range allows lower $K_{Hz,}$ and as shown above induced phase noise power is directly proportional to K_{Hz}. These factors can allow an extremely low noise discrete VCO to sometimes offer a superior noise solution at medium offsets, and quite often at far out offsets.

Converting Phase Noise to Time Jitter

The basic mathematics for converting between phase noise density, phase noise rms over a band, and time jitter rms, are as follows (Ref. 4). These formulas are often useful in converting given specs or CAD program outputs to other units for various calculations. The time domain form is often used in specifying low noise clocks, such as are needed in software radio applications with very high speed AD and DA clocks.

Integrated phase noise over the band of interest in radians rms is:

Equation 15: $$\boldsymbol{\varphi_{rms}(rad)} = \sqrt{\int_{f1}^{f2} \mathbf{2}\boldsymbol{L(f)df}} = \sqrt{\int_{f1}^{f2} \boldsymbol{S_\theta(f)df}}$$

For communications systems, the limits of integration are over the band where the information carrying sidebands lie. $S_\theta(f)$ is the spectral noise density on both sides of the carrier added together. L(f) and S(f) are linear (not dB).

Integrated phase noise in degrees rms is given by:

Equation 16: $$\boldsymbol{\varphi_{rms}(deg)} = \frac{\mathbf{360}}{\mathbf{2\pi}}\ \boldsymbol{\varphi_{rms}(rad)}$$

The time jitter caused by phase noise at carrier frequency f_o from offset frequencies f_1 to f_2 is:

Equation 17: $$J_{rms}(sec) = \frac{\varphi_{rms}(rad)}{2\pi f_o} = \frac{\varphi_{rms}(deg)}{360 f_o}$$

PLL simulation programs and system specifications may give integrated phase noise in any or all of the above units.

Passive Part Noises

Excess Resistor (Current) Noise: This is a noise in resistors in addition to thermal noise, and is a 1/f type noise that at a given frequency is proportional to DC current flow (Ref. 5, pp. 290-296). It is most commonly measured in µV per volt per decade, which is referred to in data sheet specs as the Noise Index NI of the resistor. The "current" referred to is not thermal noise current, but DC bias current leading to a shot type noise. However, it is not ideal shot noise. It is a noise due to resistive particles touching in a less than perfect way so that current flow is not evenly distributed. Low cost thick film resistors have higher excess noise, and thin film have lower noise at still attractive pricing (<$0.10 each). Metallic has the lowest noise of all, but is less available and much more expensive (approximately $4 to $8 each in foil form).

The seemingly odd definition of excess noise on a per decade basis instead of a per root Hz density basis is due to convenience in calculation, where the 1/f nature of the noise power results in each decade of frequency having the same noise power. For example, if a range of frequency from 1kHz to 100kHz is of interest, this is two decades. It has twice the total noise power of a single decade, and thus it has 1.414 the noise voltage of a single decade. If a resistor has noise index of 1µV per volt and is biased at 2V, it has 2µV of excess noise per decade. In two decades it will have 2µV X 1.414 = 2.83µV.

The spectral noise density due to excess noise is normally how we would work with it in PLL design. This is not made clear in Ref 5, so it is derived here, as follows. It is given that excess noise power is 1/f. Thus:

Equation 18: $$P_{ne} = \frac{n^2}{f}$$

Here "n" is a proportionality factor for actual noise voltage density. In the above P_{ne} is the actual noise power density taking V_{DC} into account. Let $\mathbf{E_{nf}}$ be the "excess noise factor", or noise V_{rms} per V_{DC} per decade that is normally specified. Note E_{nf} = NI X (1E-6) since NI is given in units of µV per V per decade. Then noise power per decade N_{pd} and n are related by:

Equation 19: $$\mathbf{N_{pd}} = E_{nf}^2 V_{DC}^2 = \int_{\mathbf{f}}^{\mathbf{10f}} \mathbf{P_{ne}}\,\mathbf{df} = \int_{\mathbf{f}}^{\mathbf{10f}} \frac{\mathbf{n^2}}{\mathbf{f}}\mathbf{df} = \mathbf{(n^2)ln(10) = 2.3(n^2)}$$

Then,

Equation 20: $$n = 0.659\, E_{nf} V_{DC}$$

Then the desired spot noise voltage density V_{ne} as a function of E_{nf} = NI X 1E6 is given by:

Equation 21: $$V_{ne}(f) = \frac{n}{\sqrt{f}} = \frac{0.659\, E_{nf} V_{DC}}{\sqrt{f}} = \frac{0.659\, E_{nf}\, R\, I_{DC}}{\sqrt{f}}$$

Now this spectral density may be used in our noise calculations, if we find we must use resistors with current flow. It would generally be better not to even allow this resistor current flow and have to suffer this additional noise source, as excess noise has quite a bit of variability and will become larger than thermal noise at a cross-over frequency generally between 1kHz and 10kHz. If we must have this noise source, it is minimized with smaller thin film resistor values in larger physical packages. The larger packages also allow lower resistor values due to their higher power dissipation.

To illustrate this, let us consider a realistic example for a buffered loop filter. This is a less recommended but still common loop filter form where a non-inverting amplifier is embedded in a loop filter to provide DC gain to control a VCO with a tune range greater than the charge pump can provide. In the non-inverting form, the gain setting resistors carry a DC current. With a very low noise discrete VCO, an optimum bandwidth might be about 10kHz (this will be shown in Part 3), so we are interested in the resistor excess noise density at 10kHz. Vishay provides a line of high grade thin film resistors that they have characterized for excess noise. The noise index of these resistors is about 0.04 µV/V per decade, leading to E_{nf} for the above equation of 4.0E-8. Let us assume an op amp can safely provide 5mA of current in DC flow to the gain set resistors and that 10V max output is required, needing a gain of 3.5 from the charge pump output. The series combination of the gain set resistors will be 2k, and from the required gain the forward resistor is ideally 1429 ohms and back resistor 571 ohms. The thermal and excess noise of the forward resistor goes straight to the op amp output. The thermal noise of the forward resistor is 4.78nV per root Hz, and the excess noise at 10kHz is 1.88nV. The back resistor, since its noise is gained, will generate the same amount (derivation outlined in filter analysis section). While the excess noise is smaller than thermal in this case, it is definitely not negligible. It is larger than the noise of a very low noise op amp.

For a particular resistor technology in a particular design case we may define a cross-over frequency below which the excess noise is larger than the thermal noise. We find a relationship by setting thermal noise power equal to excess noise power and solving for f, which yields:

Equation 22: $$f_{ex-cross} = \frac{0.1085 E_{nf}^2 I_{DC}^2 R}{kT}$$

For the example given above, a resistor featuring low excess noise, the cross over frequency is 1593Hz. For a thick film resistor it would usually be higher. At this frequency there will be a 3dB increase in resistor noise, and as frequency drops noise power is rising 1/f. In a lower bandwidth PLL this 1/f source can be noticeable.

Ceramic Capacitor Noise: COG/NPO capacitors are nearly noise free, but commonly available only for 0.1µF and lower. High dielectric constant capacitors, such as X5R, X7R, and Z5U, are available in much larger values, up to about 10µF for 1206. But, these dielectrics are piezoelectric and can generate noticeable noise voltage in high vibration environments. In

typical lab environments, the author's analysis indicates that such noises are typically not noticeable. Analysis is conducted in terms of quantifying the mechanical to electrical noise conversion properties of the capacitors. Mechanical noise is quantified spectrally in terms of g^2/Hz or g/rootHz, and conversion from this input to charge/voltage output is a function of dielectric. Careful investigation and analysis would be needed to use these caps in noise sensitive spots in applications such as vehicular and aircraft radios. When a high dielectric ceramic capacitor is exposed to real mechanical stress, its noise is striking. Tapping a large value cap while monitoring its voltage on an oscilloscope can show millivolts of noise.

Tantalum Capacitor Noise: Tantalum has low cost and high volumetric efficiency. It also has less microphonic noise than high dielectric constant ceramics for noise filtering in high vibration environments. But, it suffers both highly variable flicker noise, and leakage of about 0.01 μA/μF/V at room temp at rated voltage.

The rather high 1/f noise of tantalum capacitors is not commonly familiar to engineers. However, there have been several published studies on the issue (Refs 6-7). The literature reports that this noise is both surprisingly large and also quite variable. For example, the data in Ref. 6 can be distilled down to giving an approximate range of the noise current in the tantalum as about 2E-15 A/μF/V to 2E-13 A/μF/V, at 10Hz at room temperature. Passing this current through the impedance of the capacitor, at 3V at 10Hz, this would be a noise voltage range of about 1nV to 100nV. It gets considerably worse at high temperatures, as much as 5X to 10X worse, and its variation can be as much as the 4^{th} power of voltage. So, we might expect this noise voltage have a typical range of about 5nV to 500nV over temperature at 10Hz, and more than this at higher voltages. In comparison, the noise of a Texas Instruments OPA1611 op amp at 10Hz is about 3nV.

The first time the author encountered this noise, he contacted several prominent low noise experts and authors about it. The conclusion was that almost nobody is aware of it. Since it is dominant only at fairly low frequencies, the power supply rejection of op amps is able to adequately cope with it, and it is often unaccounted for. However, if using a tantalum in an RC noise filter where the powered device does not have excellent PSRR, then it can easily be a problem. Before being aware of this noise, the author had blindly gotten away with using tantalum for noise filtering in an application where film caps were too large and too expensive. But, that was just luck. A different part, a different manufacturer, or higher temps and voltages could have easily been a different story.

Film Capacitor Noises: Film capacitors are lower noise than tantalum, and with low microphonics. Though film caps are not piezoelectric, compression of plate spacing with a fixed charge can result in modulation of capacitor voltage.

The only reference on film capacitor noise the author is aware of is Ref 8. It is pointed out there that the nature of this noise is random voltage change on the order of 10 μV to 300μV. The cause of these voltage spikes is energy released that has been dielectrically absorbed. It is apparently not a commonly experienced problem because the mean time between such spikes varies over a large amount of time, from seconds to years. It is more common during temperature change events. A noise voltage of this magnitude is very large compared to the noises we are used to working with in low noise synthesizer design, but fortunately these are rare in occurrence.

From this work, the noise generation of plastic film caps from lowest to highest is in this order:

1. Polystyrene (very little availability)

2. Polypropylene (about $0.4 to $0.6 per µF at 1000 units)
3. Parylene
4. Polyethylene (more cost effective "metel-polyester" caps fall in this group, at about $0.10 to $0.20 per µF at 1000 units)
5. Teflon
6. Polysulfone
7. Polycarbonate
8. Mylar (technically BoPET (Biaxially-oriented polyethylene terephthalate), a polyester film made from stretched polyethylene terephthalate)

Filter Noises and Limits

Noise in the loop filter is for the most part servoed out well inside the loop bandwidth, as will be later shown. But, around the loop bandwidth and for up to a decade or so past the loop bandwidth, the noise of the filter may dominate the phase noise. It was shown earlier how the minimum induced noise is given by R_2 thermal noise, and that his noise power is proportional to the product of loop bandwidth f_L and VCO gain K_{Hz}. As loop bandwidth is directly proportional to R_2 and other resistors in the passive loop filter generally scale with R_2, the filter noise may set limits on the bandwidth to be used in the PLL. The active loop filter has the advantage that the largest resistor noise will generally be from R_2, but the disadvantage of op amp and reference noises. In the active filter case, the noise current of the op amp also flows through R_2, and this can be an even worse noise source than the thermal noise of R_2. In analyzing the noises of the main filter cases, we shall pause at several points to evaluate the limits on loop bandwidth if we do not wish further noise degradation.

Second Order Passive Filter Noise: The 2nd order passive filter has the form shown in Figure 2.

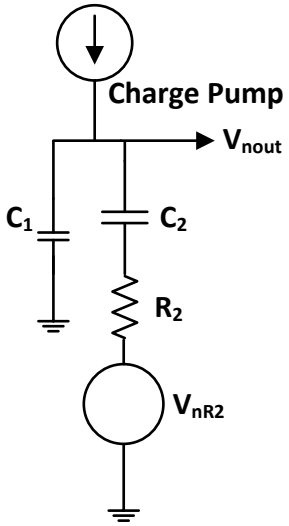

Figure 2: The 2nd order loop filter with its single internal noise source, the thermal noise in R_2.

Analysis of the above circuit yields:

Equation 23: $$|V_{noutR2}|^2 = \frac{4kTR_2}{\left(1+\frac{C_1}{C_2}\right)^2+(2\pi f R_2 C_1)^2}$$

The filter impedance Z_f as seen by the charge pump is:

Equation 24: $$Z_f = \frac{sC_2R_2+1}{s(sC_1C_2R_2+C_1+C_2)}$$

If the noise of the charge pump and dividers is modeled as a noise current I_{pn}, then:

Equation 25: $$|V_{ncp}|^2 = I_{pn}^2 |Z_f|^2 = I_{pn}^2 \frac{\omega^2 C_2^2 R_2^2 + 1}{\omega^4 R_2^2 C_1^2 C_2^2+\omega^2(C_1+C_2)^2}$$

The total filter noise squared is then the sum of these two noises. This form of loop filter is the lowest possible noise, as it only has R_2 as an internal noise source. This equation may be reused for the R_2 noise term in the slow slew active loop filter also.

Third Order Passive Filter Noise: The 3rd order passive loop filter is shown in Figure 3. Getting V_{nout} from the contribution of both V_{nR1} and V_{nR3} is a worthy algebraic challenge. To tackle it we define several intermediate impedances. For example, $Z_{3\text{-}1}$ is the impedance of C_1 in parallel with the series impedance of R_3 and C_3. $Z_{2\text{-}1}$ is the impedance of C_1 in parallel with the series impedance of R_2 and C_2. We then apply voltage and current division to the different blocks. For example, the noise voltage V_{nR1} divides over $Z_{3\text{-}1}$ and Z_2 to give a voltage on C_1. That voltage then divides over C_3 and R_3 to give the noise voltage on C_3 from V_{nR2}.

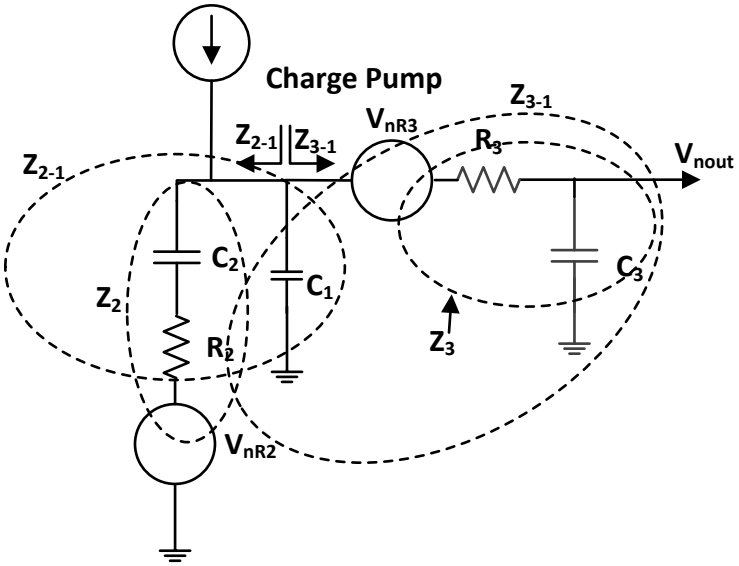

Figure 3: Third order passive loop filter with intermediate impedances defined for finding V_{nout}.

Going through this process, we find the below set of equations.

Equation 26: $$\boldsymbol{Z_f(s) = \frac{1+sT_2}{s\,A_0(1+sT_1)(1+sT_3)} = \frac{1+sC_2R_2}{s\left(A_2\,s^2+A_1\,s+A_0\right)}}$$

Equation 27: $$\boldsymbol{T_2 = R_2C_2}$$

Equation 28: $$\boldsymbol{T_3 = R_3C_3}$$

Equation 29: $$\boldsymbol{T_{3-1} = \frac{C_1C_3}{C_1+C_3}\,R_3}$$

The noise from R_2 at the output is:

Equation 30: $$\boldsymbol{V_{nout2} = \frac{4kTR_2}{\frac{C_1+C_3}{C_2}(sT_2+1)(sT_{3-1}+1)+(sT_3+1)}}$$

The noise from R_3 at the output is:

Equation 31: $$\boldsymbol{V_{nout3} = \frac{4kTR_3\,[C_1(sT_2+1)+C_2]}{(sT_3+1)[C_1(sT_2+1)+C_2]+C_3(sT_2+1)}}$$

And then finally,

Equation 32: $$\boldsymbol{V_{nout} = \sqrt{V_{nout2}^2 + V_{nout3}^2}}$$

In older integer N designs with much larger value of N, R_3 would usually be much greater than R_2 and thus quite noisy. This was partially due to older design methods where the methods for calculating R_3 and C_3 were not as well developed, and a large R_3 was typically chosen to make it easy not to load the passive loop filter. In the modern method the effect of R_3 and C_3 on loop phase margin are fully taken into account and quite well controlled, and a smaller value of R_3 is typical. Both R_2 and thus R_3 are also smaller with the lower N value of modern fractional N synthesizers with high phase detector frequencies. Often R_3 is in the range of about R_2 to 3X R_2. We may thus roughly approximate the noise voltage to expect from the properly designed 3rd order passive loop filter to be about 1.5 to 2X that of the 2nd order filter. In the case of the integrated VCO with relatively high noise compared to a discrete VCO, this noise is often negligible. In the very low noise discrete VCO case, it is more likely to be noticeable. This lower R_2 and R_3 value, along with higher frequency to be divided down to the

application frequency, and the higher phase detector frequency and loop bandwidth of the modern sigma delta PLL as will be presented in article 3, are all essential factors in lower total noise.

The noise from the 3rd order passive filter is manageable for calculations if coded in a program like Excel or Mathcad. For the 4th order passive filter, the author would recommend SPICE simulation of this noise. It is quite simple to check filter noise with SPICE, and it is also possible for a behavioral model of the entire loop to be built in SPICE. However, even a model complete enough to show just the quasi-linear phase locked mode, and not the non-linear frequency lock mode, requires what might be called tricky methods. For example, most SPICE versions do not include a simple 1/f noise source that could be used to generate VCO, crystal reference, and synthesizer IC 1/f noises. These SPICE versions thus require knowing how to force the particular SPICE version to generate a 1/f noise source, and these methods vary between versions.

Third Order Buffered Semi-Active Filter: A common active filter strategy is to break the 3rd or 4th order passive filter up with an op amp buffer in the middle, which shall be referred to here as "semi-active". This can be beneficial if the noise of R_3 is noticeable in the passive filter case, if moderately greater tune voltage is needed, or if VCO input leakage current is on the large side. The op amp allows for a much lower value of R_3 with negligible thermal noise, or for two low impedance stages after the op amp with considerably simpler design than having two stages of filtering right on the passive filter. The possible gain used for higher tune voltage of course gains up noise of the op amp as well, but if this gain is limited the noise may be acceptable. However, implementing the gain does add more noise, and since there is DC current flow in these resistors excess noise is also introduced. The circuit is shown in Figure 4.

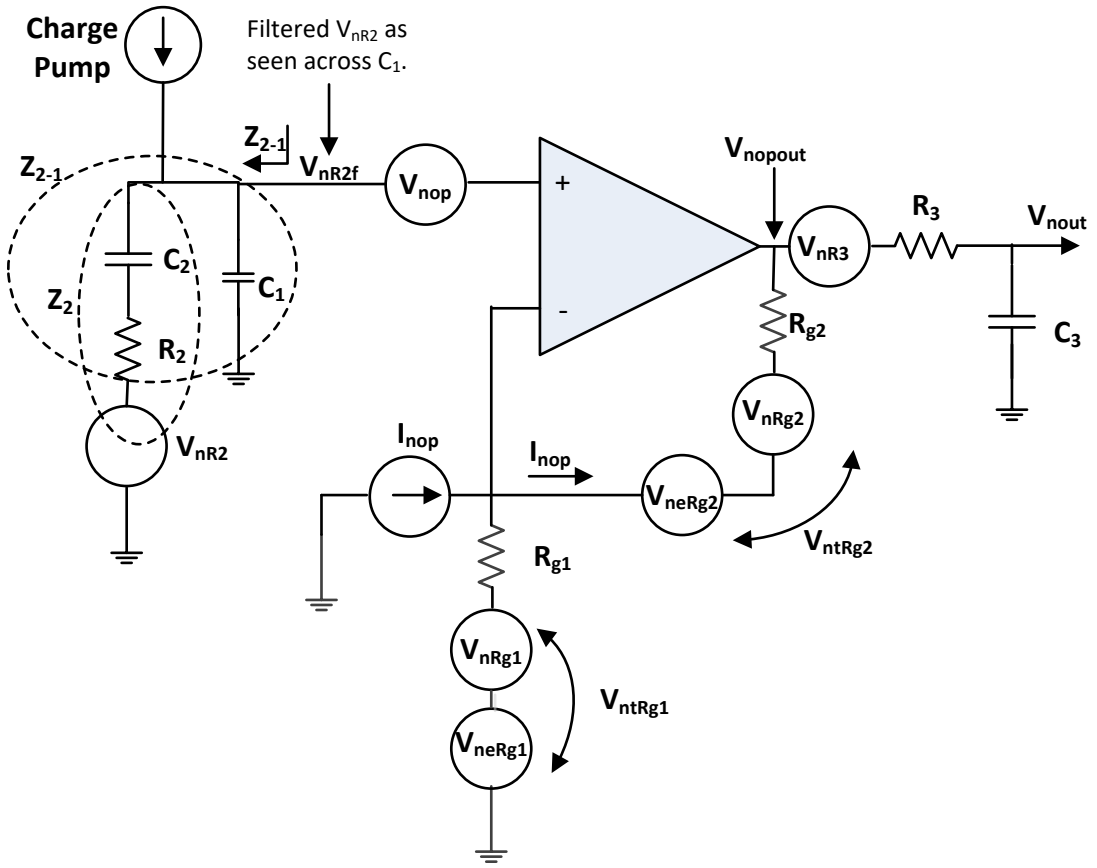

Figure 4: Buffered 3rd or 4th order semi-active filter. For 4th order, an additional RC stage is added after R_3-C_3.

The noise from resistor R_2, which shall be here called V_{niR2}, on the op amp input, has been given before as the noise from the 2nd order filter. V_{nop} is rms summed with V_{niR2} to get the total noise voltage on the op amp plus input. That noise is then gained to the op amp output by $(1 + R_{g2}/R_{g1})$. The op amp current noise I_{nop} is forced by feedback to flow totally in R_{g2} in order to maintain the two op amp inputs as the same voltage. The rms sum of resistor R_{g2} thermal noise V_{nRg2} and excess noise V_{neRg2} goes straight to the op amp output, again forced by the feedback conditions. The rms sum of resistor R_{g1} thermal noise V_{nRg1} and excess noise V_{neRg1} is gained to the op amp output by R_{g2}/R_{g1}. For convenience we may include the noise of R_4 as part of the noise on the op amp output. We may thus write the noise voltage on the op amp output as:

Equation 33:
$$V_{noptot}^2 = \left[V_{nR2}^2 + V_{nop}^2 \right] \left(1 + \frac{R_{g2}}{R_{g1}} \right)^2 + V_{nRg2}^2 + V_{neRg2}^2 + \left(V_{nRg1}^2 + V_{neRg1}^2 \right) \left(\frac{R_{g2}}{R_{g1}} \right)^2 + i_{nop}^2 R_{g2}^2 + V_{nR4}^2$$

This noise needs merely to be passed through a noiseless R_3-C_3 filter to give the noise from the active filter to be presented to the steering input of the VCO.

Equation 34: $$V_{nout}^2 = \frac{V_{noptot}^2}{\omega^2 C_4^2 R_4^2 + 1}$$

An interesting feature of this architecture is that if the two gain resistors have the same noise index, then the excess resistor noise from each of R_{g2} and R_{g1} in the op amp output is identical. Recall the equation for noise density per Hz that was developed earlier from the normally specified noise index of µV per V per decade of frequency:

Equation 35: $$V_{ne}(f) = \frac{n}{\sqrt{f}} = \frac{0.659\, E_{nf} V_{DC}}{\sqrt{f}} = \frac{0.659\, E_{nf}\, R\, I_{DC}}{\sqrt{f}}$$

The two resistors have the same DC current flow, and the excess noise of each is proportional to its value. The noise from R_{g2} comes straight to the output. The noise from R_{g1} is gained by R_{g2}/R_{g1}, hence its proportionality factor R_{g1} is canceled and replaced by R_{g2}. The two excess noise powers are thus identical.

Because of the extra noise added by gain and by the thermal and excess noise of the gain resistors, using this circuit with gain is not highly recommended, though it is a fairly common practice if the noise does not have to be the very best. When used in unity gain mode, it may well save a few dB's of noise around the loop bandwidth by replacing the noise of a larger R_3 with op amp noise as low as about 1nV.

Fourth Order Active Filter Noise: The design methodology for the "slow slew mode" 4th order active filter was given in the first article of this series. This active filter architecture is designed to reduce the bandwidth and slew rate requirements on the op amp, at which it is partially successful. The use of the inverting mode with R_2 and C_2 in the feedback path allows this form to provide higher tune voltages with low noise gain. Current flows through R_3 and then through R_2-C_2 to charge up the op amp output to whatever voltage is needed. The input RC is intended to shield the op amp from the high slew rate and bandwidth of the charge pump output.

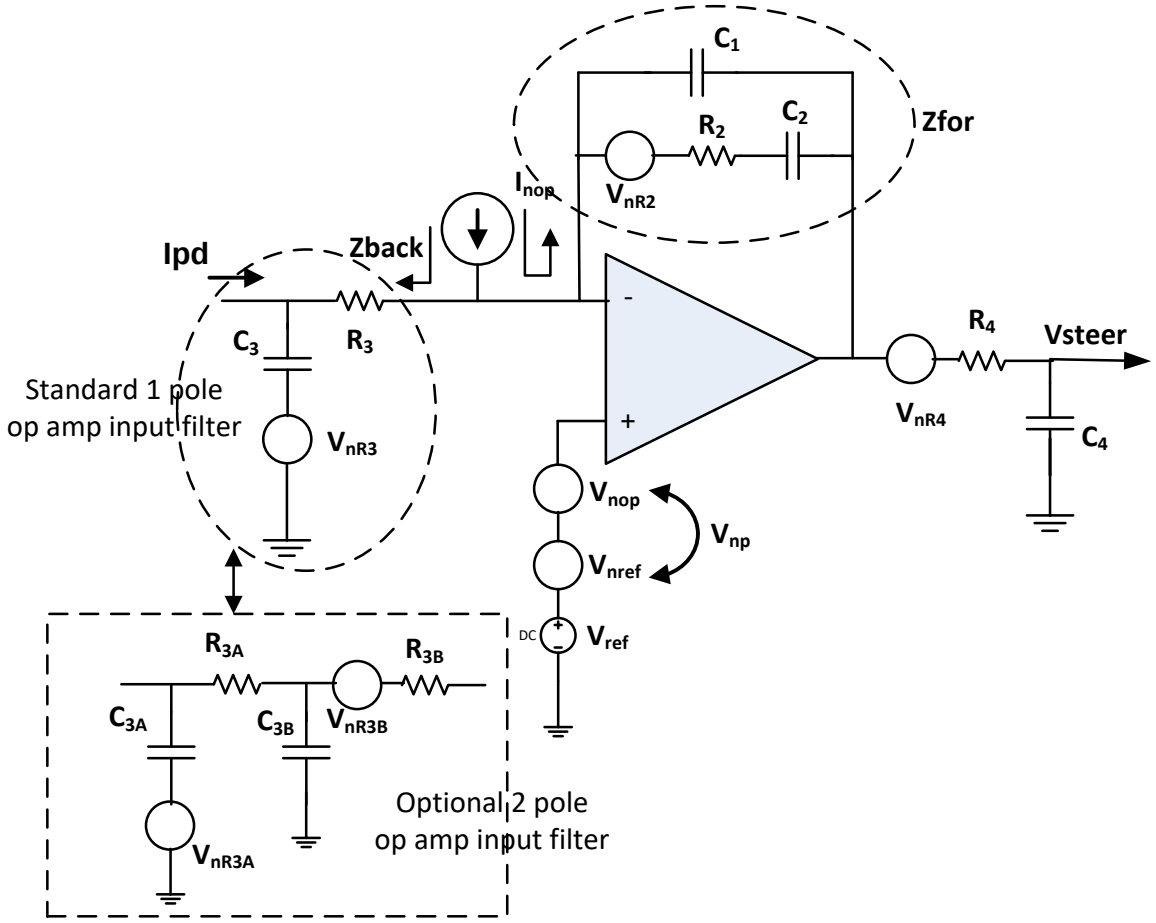

Figure 5: The 4th order active loop filter with option to become 5th order. The noise sources to be analyzed are shown.

However, despite its benefits in limiting the op amp's exposure to high frequency signals from the charge pump, it may be advantageous to add an additional input RC stage to further protect the op amp from high speed signals. The single pole input stage still has steps in the voltage on C_3 that have ramp times equal to the pulse width of the phase detector output, which with modern synthesizer chips is about 0.5ns to 1ns. The repetition rate on these pulses with modern synthesizer IC's is often 100 to 200MHz, which is well beyond the bandwidth of most very low noise op amps. The second input stage will smooth these considerably, as later SPICE simulation in Part 5 with examples will show. As pointed out by Banerjee, experimental evidence (Ref. 9, 5th ed., pp.371-372) indicates that the op amp in an active loop filter not being fast enough sometimes seems to cause a several dB rise in the 1/f noise of the PLL, presumably due to pulse widening allowing through more charge pump 1/f noise. Though this issue is not fully settled at the time of this writing, it would make logical sense that an additional input pole to keep most of the frequency content of the phase detector pulses inside the op amp bandwidth would be of help in avoiding this low frequency degradation.

The noise on steering output of the active filter may be characterized as the sum of the noise powers from the plus input, from the minus input, from the forward impedance, and in the final RC stage.

The minus input noise is the thermal of R_3, gained up by:

Equation 36: $$V_{nopR3}^2 = 4kTR_3 \left|\frac{Z_{for}}{Z_{back}}\right|^2$$

We can generate this over frequency using the next several relationships. Normally we use the square relationships to add powers, and convert summed power back to noise voltage as the final step.

Equation 37: $$Z_{back} = R_3 + \frac{1}{sC_3R_3} = \frac{sC_3R_3+1}{sC_3}$$

Equation 38: $$Z_{for} = \frac{1+sR_2C_2}{s(C_1+C_2+sR_2C_2C_1)}$$

Next, we consider the gained noise from the plus input of the op amp. This is the gained rms sum of the reference noise and the op amp's own noise, given by:

Equation 39: $$V_{nopp}^2 = V_{np}^2 \left|1 + \frac{Z_{for}}{Z_{back}}\right|^2$$

The below magnitude squared functions are convenient to use.

Equation 40: $$|Z_{back}|^2 = R_3^2 + \frac{1}{\omega^2 C_3^2} = \frac{\omega^2 R_3^2 C_3^2 + 1}{\omega^2 C_3^2}$$

Equation 41: $$\left|Z_{for}\right|^2 = \frac{\omega^2 C_2^2 R_2^2 + 1}{\omega^4 R_2^2 C_1^2 C_2^2 + \omega^2 (C_1+C_2)^2}$$

A word of warning is appropriate here. It is common practice for the plus input reference voltage to be provided by a divider chain with a capacitor on the plus input for noise filtering. But, such a divider chain will have current flow and thus will suffer from the excess noise described above. Avoiding such a chain with an ultra-low noise reference is preferred, but if a divider must be settled for, it should at least be thin film resistors and not thick film. Metal foil resistors are a lower noise option, but they are quite expensive and for similar cost a very low noise reference can be directly provided (Part 4).

The noise generated by R_2 is found taking into account that the minus input of the op amp is a "virtual ground". Op amp feedback holds it equal to the plus input, so noise from R_2 comes straight through to the output, except for being filtered within Z_{for} when $C_1 > 0$. It's the same relation as was found for the noise in the 2nd order passive filter.

Equation 42: $$\left|V_{nopR2}\right|^2 = \frac{4kTR_2}{\left(1+\frac{C_1}{C_2}\right)^2 + (2\pi f R_2 C_1)^2}$$

The noise generated on the op amp output by the op amp noise current is again found by noting that the minus input is kept equal to the plus input by op amp feedback. The only way for that to hold is for I_{nop} to flow totally through Z_{for} and not through Z_{back}.

Equation 43: $$\left|V_{nopInop}\right|^2 = I_{nop}^2 \left|Z_{for}\right|^2$$

For the sake of convenience, we may count the noise of R_4 as part of op amp output. We now have all the noise terms at the op amp output.

Equation 44: $$V_{noptot}^2 = V_{nopR3}^2 + V_{nopp}^2 + V_{nopR2}^2 + V_{nopInop}^2 + V_{nR4}^2$$

This noise needs merely to be passed through a noiseless R_4-C_4 filter to give the noise from the active filter to be presented to the steering input of the VCO.

Equation 45: $$V_{nout}^2 = \frac{V_{noptot}^2}{\omega^2 C_4^2 R_4^2 + 1}$$

With the above we have all the major open loop noises to be shaped by the loop except for what is sometimes called the "PLL noise". This is something of a misleading term, since it typically means just the noise of the charge pump and dividers in the synthesizer IC, not the total PLL noise. It is not given above in the noise sources review as it is normally specified as a closed loop noise after shaping. It will be covered in the next article along with the methods for analyzing how noise is shaped, optimum loop bandwidth, and the synthesizer IC figure of merit for evaluating chip noise.

About the Author: Farron Dacus is an RF design consultant in Dallas, Texas. His BSEE and MSEE are from the University of Texas, and he has over 30 years of experience ranging from IC's to circuits to systems in low noise RF, short range radio / IoT, cellular, military communications, and aircraft radios. He may be reached at farron.dacus@longwingtech.com.

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