Design Feature

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Design Methods of Modern Ultra-Low-Noise Synthesizers

This first article in a multi-part series on modern synthesizers describes basic phase-locked-loop operation along with various topologies.

Recent years have seen major changes in frequency-synthesis art. Ultra-low-noise discrete voltage-controlled oscillators (VCOs), the heart of low-noise synthesizers for decades, now find themselves being challenged by integrated VCOs. While the best discrete VCOs still achieve 20 to 30 dB of phase-noise superiority, integrated-circuit (IC) companies are conducting an asymmetric battle to dominate the market with full integration based not on the best VCO noise, but on architectural innovations that often render free-running VCO noise less important.

Such a goal is achieved by putting good VCOs on die, suppressing that noise down to a very low level via feedback, and then dividing down to the application band. The challenge that discrete VCO suppliers now face is to extend the outstanding phase noise they achieve in application bands to higher frequencies, where they also get the full architectural benefit of the latest synthesizer innovations.

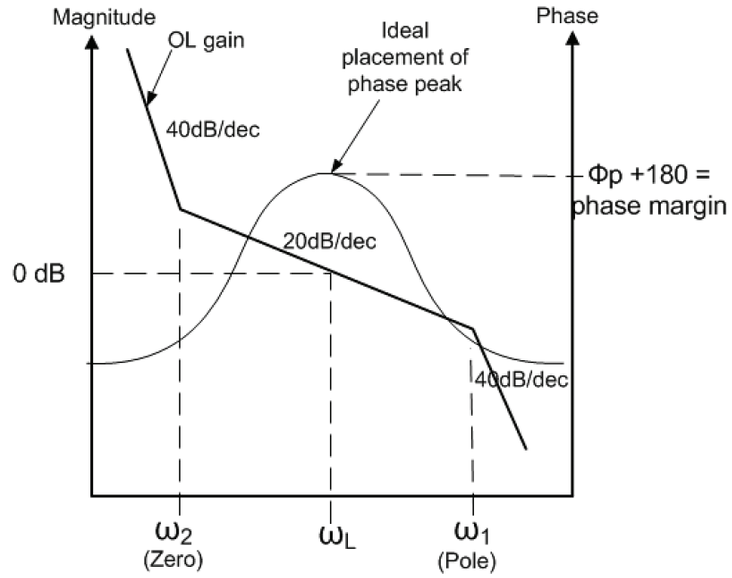
This article, the first of a four-part series, will review modern advanced design methods. The next three articles will dive into noise, key parts and tools, and examples. Longer and more complete versions of these articles will be published online.

BASIC PLL OPERATION AND SECOND-ORDER NORMALIZED FORM

The standard second-order form of phase-locked-loop (PLL) design that's presented in most classic textbooks allows for approximate, but still useful, design and analysis equations, along with a simple description of loop operation *(Fig. 1)*.

We are accustomed to thinking primarily of voltage and current as the feedback quantities. But in addition to those, the PLL treats phase and frequency as small-signal frequency-domain variables. When seeking lock over a wide frequency range, the modern phase/frequency detector (PFD) acts as a frequency detector to steer the VCO toward lock. As frequency converges, the loop transitions to a phase-locked mode where phase as a time difference between digital edges is driven to zero.

1. This is a depiction of the second- and third-order charge pump PLL synthesizer ($C_1 = 0$ for second-order). Frequency is set by firmware via the programmable R and N dividers.



2. Shown is open-loop gain and phase in the properly designed third-order PLL. The maximum phase is forced to occur at the loop bandwidth by the design.

Since frequency is the time derivative of changing phase (ω = dθ/dt), phase is the integral of frequency. Thus, the VCO acts as an integrator of input voltage to output phase, which introduces −90 degrees of phase shift. That's why its transfer function is in the form K_o/s. Here, K_o is given in units of rad/sec/volt. VCO datasheets will normally give K_o in units of MHz/V. To be clear in this article series, we will refer to the Hz/V form of K_o as K_{Hz}. The radian form will be referred to as K_o, i.e., $K_o = 2\pi K_{Hz}$.

With the −90 deg phase shift and the −180 degrees of negative feedback, we are only allowed a maximum of 90 degrees of filtering phase shift before −360 degrees total results in instability. We normally leave a minimum of 40 degrees of "phase margin" at the loop bandwidth. This margin comes from the zero introduced by resistor R_2, as without it the charge pump driving a capacitor would also be an integrator.

From basic analysis of the loop in *Fig. 1*, we may find R_2 and C_2 as:

$$C = \frac{K_o I_{pd}}{2\pi N \omega_n^2} = \frac{K_{Hz} I_{pd}}{N \omega_n^2} \quad (1)$$

$$R = \frac{4\pi N \omega_n \zeta}{K_o I_{pd}} = \frac{2N\omega_n\zeta}{K_{Hz} I_{pd}} \quad (2)$$

The term ω_n is the "natural" frequency (settling "ring down" frequency). It's close to the open-loop bandwidth. The term ζ is the "damping factor" and must be greater than zero for stability (usually set at 0.5 to 1.0). See the online version for a derivation of the above and a more complete description.

THE THIRD-ORDER PASSIVE FILTER PLL

This third-order passive filter PLL is the simplest highly usable form. It's realized by adding another capacitor *(Fig. 1)*. Introducing another filter pole will eventually cancel out the zero. This means that there will be a frequency where phase peaks and then declines *(Fig. 2)*.

The loop filter impedance is:

$$Z(s) = \frac{1+sT_2}{s\,A_0(1+sT_1)} \quad (3)$$

A half page of circuit analysis will establish:

$$T_2 = R_2 C_2 \quad (4)$$

$$T_1 = \frac{R_2 C_2 C_1}{A_0} \quad (5)$$

$$A_0 = C_1 + C_2 \quad (6)$$

The open-loop gain function is given by (*see figure for G and H*):

$$\mathbf{GH(j\omega)} = \frac{K_d K_o}{-N} \frac{1+j\omega T_2}{\omega^2 A_0 (1+j\omega T_1)} \quad (7)$$

We know K_d, K_o, and N, and choose loop bandwidth ω_L and phase margin ϕ_m. To find our three unknowns A_0, T_1, and T_2, we need three equations. We get them from the magnitude of GH (which is 1 at ω_L), the phase of GH (which gives ϕ_m at ω_L), and the derivative of the phase of GH with respect to ω (which is zero at ω_L). This is the basic methodology referred to here as the modern technique.

The magnitude of GH is:

$$|GH(j\omega)| = \frac{K_d K_o}{N A_0 \omega^2} \frac{\sqrt{1+\omega^2 {T_2}^2}}{\sqrt{1+\omega^2 {T_1}^2}} \quad (8)$$

At $\omega = \omega_L$, this magnitude is 1, and we have:

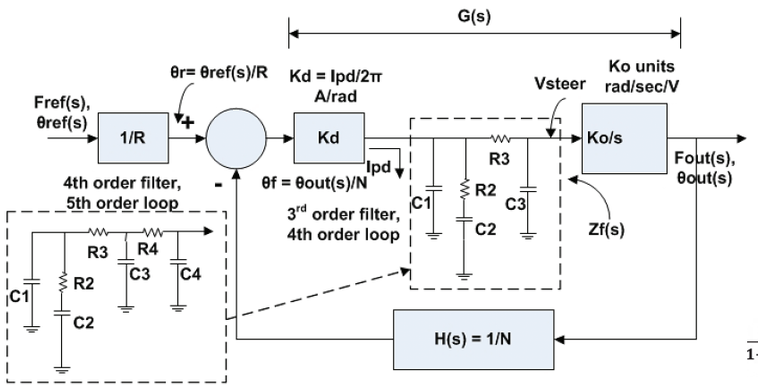
$$A_0 = \frac{K_d K_o}{N\omega_L^2} \frac{\sqrt{1+\omega_L^2 {T_2}^2}}{\sqrt{1+\omega_L^2 {T_1}^2}} \quad (9)$$

The phase *margin* expressed as a positive number from 0 to 90 degrees is the difference between the open-loop phase and 180 degrees, which is:

$$\phi_m = \tan^{-1}(\omega_L T_2) - \tan^{-1}(\omega_L T_1) \quad (10)$$

Taking the derivative of phase margin with respect to variable frequency, and setting it to zero at $\omega = \omega_L$, gives:

$$\frac{T_2}{1+\omega_L^2 T_2^2} - \frac{T_1}{1+\omega_L^2 T_1^2} = 0 \quad (11)$$



3. Here are the fourth- and fifth-order PLL forms.

We now have two nonlinear equations in the two unknowns T_1 and T_2. We may solve these numerically, but there's a closed form solution (Ref. 1, pp. 32-36):

$$T_1 = \frac{\frac{1}{\cos\phi_m} - \tan\phi_m}{\omega_L} \quad (12)$$

$$T_2 = \frac{1}{\omega_L^2 T_1} \quad (13)$$

$$\omega_L = \sqrt{\omega_1 \omega_2} \quad (14)$$

Now we may find the circuit values:

$$C_2 = A_0\left(1 - \frac{T_1}{T_2}\right) \quad (15)$$

$$C_1 = A_0 - C_2 \quad (16)$$

$$R_2 = \frac{T_2}{C_2} \quad (17)$$

The second-order filter is the lowest noise filter form. However, pushing bandwidth out typically requires additional poles of filtering to keep phase detector noise from contaminating VCO noise.

THE FOURTH-ORDER PASSIVE FILTER PLL

The fourth-order passive filter PLL form uses the third-order filter shown in *Figure 3*. It's likely the most common filter form.

The open-loop transfer function is given by:

$$\mathbf{GH(j\omega)} = \frac{K_d K_o}{-N} \frac{1+j\omega T_2}{\omega^2 A_0(1+j\omega T_1)(1+j\omega T_3)} \quad (18)$$

The filter (transfer) impedance that's part of the above is given by:

$$Z(s) = \frac{1+sT_2}{s\,A_0(1+sT_1)(1+sT_3)} = \frac{1+sC_2R_2}{s\,(A_2 s^2 + A_1 s + A_0)} \quad (19)$$

The coefficients A_1 and A_2 are useful abbreviations for lengthy functions of parts values.

$$A_0 = C_1 + C_2 + C_3 \quad (20)$$

Using the magnitude function of the open-loop transfer function:

$$A_0 = \frac{K_d K_o}{N\omega_L^2} \frac{\sqrt{1+\omega_L^2 T_2{}^2}}{\sqrt{(1+\omega_L^2 T_1{}^2)(1+\omega_L^2 T_3{}^2)}} \quad (21)$$

We next define what Banerjee (Ref. 2) calls "pole ratios," which shall be selected by the designer based on factors such as spur rejection. Technically, these would be properly referred to as time-constant ratios.

$$T_{31} = \frac{T_3}{T_1} = \frac{\omega_1}{\omega_3} = \frac{f_1}{f_3} \quad (22)$$

T_{31} determines how spaced out the added pole is. We must use $T_{31} < 1$. We find that 0.5 buys almost all of the possible spur suppression.

The phase margin of the open-loop transfer function is given by:

$$\phi_m = \tan^{-1}(\omega_L T_2) - \tan^{-1}(\omega_L T_1) - \tan^{-1}(\omega_L T_{31} T_1) \quad (23)$$

The phase margin occurs at the peak of the phase margin function. Taking this derivative with variable frequency, and then applying the first derivative test with $\omega=\omega_L$, gives:

$$\frac{T_2}{1+\omega_L^2 T_2^2} - \frac{T_1}{1+\omega_L^2 T_1^2} - \frac{T_{31}T_1}{1+\omega_L^2 T_{31}^2 T_1^2} = 0 \quad (24)$$

After selecting the pole ratio T_{31}, the above two equations may be solved numerically for T_2 and T_1, thus allowing $T_3 = T_{31}T_1$.

Now we come to the "Gamma Optimization Factor" used by Banerjee. This quantity allows for approximation, with additional information on its importance given in the online version. We may extend the earlier expressions for T_2 in approximate form to higher-order loops (Ref. 2, 5th ed., p. 309), at the same time defining γ:

$$T_2 = \frac{\gamma}{\omega_L^2 (T_1+T_3)} = \frac{\gamma}{\omega_L^2 T_1(1+T_{31})} \quad (25)$$

This parameter is normally close to 1 in practical designs—in the range of 0.7 to 1.3.

Substituting, we get this approximation (leaving the 180 deg. off to convert from phase to phase margin):

$$\phi_m = \tan^{-1}\left(\frac{\gamma}{\omega_L T_1(1+T_{31}+T_{41})}\right) - \tan^{-1}(\omega_L T_1) - \tan^{-1}(\omega_L T_{31} T_1) \quad (26)$$

The above only needs to solve for T_1. An approximation can be found using $\tan^{-1}(x) \sim x$ for small x. The result is:

$$T_1 \cong \frac{\frac{1}{\cos\phi_m} - \tan\phi_m}{\omega_L(1+T_{31})} \quad (27)$$

The other two time constants follow immediately.

$$T_3 = T_1 T_{31} \quad (28)$$

When using the approximate approach:

$$T_2 \cong \frac{\gamma}{\omega_L^2 (T_1+T_3)} \quad (29)$$

We find A_1 and A_2 from:

$$A_1 = A_0(T_1 + T_3) = C_2C_3R_2 + C_1C_2R_2 + C_1C_3R_3 + C_2C_3R_3 \quad (30)$$

$$A_2 = A_0 T_1 T_3 = C_1C_2C_3R_2R_3 \quad (31)$$

We have the four equations for five values: C_1, C_2, C_3, R_2, and R_3. The method adopted by Banerjee to get a 5th equation is to find the largest C_3 that satisfies these equations. The above may be manipulated to find C_3:

$$C_3 = \frac{-T_2^2 C_1^2 + T_2 A_1 C_1 - A_2 A_0}{T_2^2 C_1 - A_2} \quad (32)$$

Applying the first derivative test for the value of C_1 that peaks C_3:

$$C_1(max\ C_3) = \frac{A_2}{T_2^2}\left(1 + \sqrt{1 + \frac{T_2}{A_2}(T_2 A_0 - A_1)}\right) \quad (33)$$

Everything needed to find C_1 is known, and it may be plugged into Equation 32 to find C_3. Then, the final values are found from:

$$C_2 = A_0 - C_1 - C_3 \quad (34)$$

$$R_2 = \frac{T_2}{C_2} \quad (35)$$

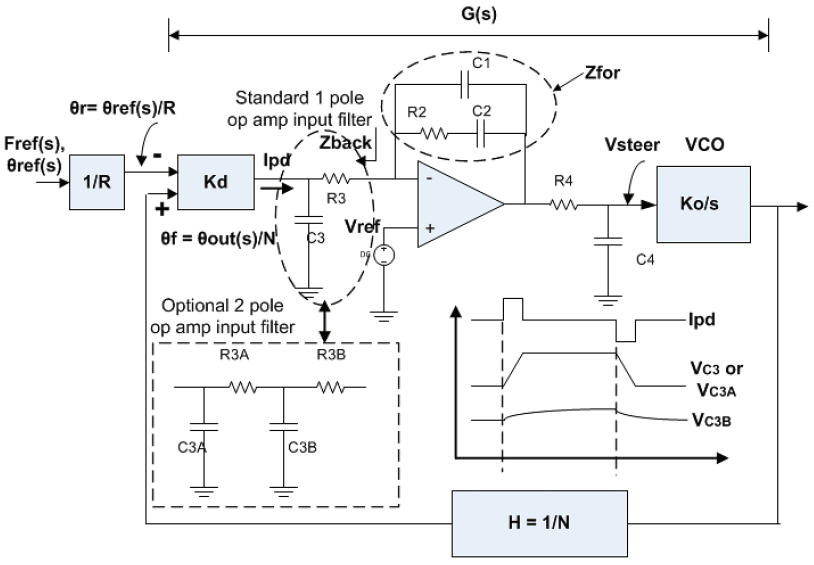
$$R_3 = \frac{A_2}{C_1 C_3 T_2} \quad (36)$$

The more complex passive fourth-order filter is discussed in the online version.

OP-AMP ACTIVE FILTER PLLs

The primary reason for using an op amp is to extend the voltage range of the loop filter so that VCOs can be controlled with large tune ranges. This allows for lower K_o and lower noise. The op amp also allows for smaller, lower-noise resistors and the ability to place the lowest pole after the op amp. Several topologies exist for active loop filters, but here a single preferred version is given in full fourth-order form *(Fig. 4)*.

A low-noise dc reference voltage is provided at the positive input of the op amp, and the combination of loop action and op-amp action will keep the negative input of the op amp at this same voltage. In this form, the op-amp output will "pump up" via current flowing through Z_{for} to assume whatever voltage is needed to maintain lock. The part values can be selected so that this inverting form suffers only small noise gain.



4. This is the active fourth-order filter and fifth-order PLL, with option for fifth-order filter. This filter is referred to as a "slow slew" active filter, as the input RC reduces speed requirements. Bandwidth limits of the op amp may still make it advantageous to use the two-pole input filter option (see online version).

For transfer impedance Z(f) we find:

$$Z(s) = \frac{V_{out}}{I_{pd}} = \frac{1+sT_2}{s\,A_0(1+sT_1)(1+sT_3)(1+sT_4)} \quad (37)$$

An importance point is that T_4 shall be the lowest frequency pole.

We also find:

$$A_0 = C_1 + C_2 \quad (38)$$

The open-loop gain as a function of jω is:

$$GH(j\omega) = \frac{K_d K_0}{-N} \frac{1+j\omega T_2}{\omega^2 A_0(1+j\omega T_1)(1+j\omega T_3)(1+j\omega T_4)} \quad (39)$$

Using the magnitude function of the open-loop transfer function (1 at loop BW), we get:

$$A_0 = \frac{K_d K_0}{N\omega_L^2} \frac{\sqrt{1+\omega_L^2 T_2^2}}{\sqrt{(1+\omega_L^2 T_1^2)(1+\omega_L^2 T_3^2)(1+\omega_L^2 T_4^2)}} \quad (40)$$

In order to maintain one set of equations whether or not f_1 or f_3 is lower, we refer both higher-frequency poles to the lowest pole f_4.

To evaluate A_0, we need T_4 and T_2; then we use the selected pole ratios to get T_1 and T_3. The exact equation is:

$$\phi_m = \tan^{-1}(\omega_L T_2) - \tan^{-1}(\omega_L T_4) - \tan^{-1}(\omega_L T_{14} T_4) - \tan^{-1}(\omega_L T_{34} T_4) \quad (41)$$

The max phase margin occurs at the peak of the phase-margin function, where we substitute $\omega=\omega_L$ after taking the derivative in the first derivative test:

$$\frac{T_2}{1+\omega_L^2 T_2^2} - \frac{T_1}{1+\omega_L^2 T_4^2} - \frac{T_{14}T_4}{1+\omega_L^2 T_{14}^2 T_4^2} - \frac{T_{34}T_4}{1+\omega_L^2 T_{34}^2 T_4^2} = 0 \quad (42)$$

Now these two may be solved numerically for T_2 and T_4, leading then to T_1 and T_3 via the selected pole ratios (usually around 0.5 for the lowest pole above f_4 and 0.25 for the next pole relative to T_4). The below approximations may be used as starting points for the numerical solutions, or as is.

$$\phi_m = \tan^{-1}\left(\frac{\gamma}{\omega_L T_4(1+T_{14}+T_{34})}\right) - \tan^{-1}(\omega_L T_4) - \tan^{-1}(\omega_L T_{14} T_4) \tan^{-1}(\omega_L T_{34} T_4) \quad (43)$$

We may use γ = 1 or alter the value from 1 based on the optimization criteria in Banerjee (Ref. 2, 5th ed., chapter 36). The only variable remaining is T_4, which may be solved numerically, or approximately:

$$T_4 \cong \frac{\frac{1}{\cos\phi_m} - \tan\phi_m}{\omega_L(1+T_{14}+T_{34})} \quad (44)$$

If the approximate form is used, then:

$$T_2 \cong \frac{\gamma}{\omega_L^2\,(T_1+T_3+T_4)} \quad (45)$$

In either case:

$$T_1 = T_{14} T_4 \quad (46)$$

$$T_3 = T_{34} T_4 \quad (47)$$

We now have all of the variables needed to find $A_0 = C_1 + C_2$. We may then find all of the part values in Z_{for} from:

$$C_1 = \frac{T_1 A_0}{T_2} \quad (48)$$

$$C_2 = A_0 - C_1 \quad (49)$$

$$R_2 = \frac{T_2}{C_2} \quad (50)$$

Now we select the values for R_3, C_3, R_4, and C_4, which seems easy as we have their time constants. But there are some subtle complexities at work here, including op-amp limits to consider.

On the input side of the op amp, it might seem like a smaller R_3 would help with noise. However, the opposite is actually true. The thermal noise of R_3 rises proportionally with its square root. But as R_3 increases, the noise gain decreases. Therefore, the noise of R_3 on the op-amp output decreases with its square root. So, we tend to select the

largest R_3 that other limits allow, as follows.

Banerjee gives (Ref. 2, 5th ed, p.38) the duty cycle of the phase-frequency detector in frequency-lock mode as a function of the ratio of f_{ref} and f_{out}/N as:

$$D_c = 1 - \frac{f_{lower}}{f_{upper}} \qquad (51)$$

In the above, f_{lower} is the smaller of f_{ref} and f_{out}/N. Since most VCOs do not steer far in a fractional sense from their center frequency, the duty cycle would seldom range above 10% (octave-type VCOs being the exception).

Let us define ΔV_{mC3} as the max filtered voltage change from V_{ref} that we wish to be imposed (such as to comply with op-amp input requirements) on C_3 during a frequency-lock acquisition event. We may thus write a relationship for R_{3max} as:

$$R_{3max} = \frac{\Delta V_{mC3}}{D_c I_{pd}} \qquad (52)$$

In addition, we need to beware of slew-rate limits. Banerjee offers experimental evidence (Ref. 2, 5th ed., pp. 371-372) that if the op amp is not fast enough, there will be worsening of 1/f phase noise inside the loop bandwidth (typically a few dB). Four slew rate cases are derived in the online version: two in frequency-acquisition mode (for lock speed) and two in PLL mode (for noise control). The worst case (highest) requirement on slew rate is usually the frequency-locking case toward the end of the frequency-lock process given by:

$$ReqSlewRateFLL(R_2\ limited) \cong \frac{D_{cmax} I_{pd}}{C_3}\frac{R_2}{R_3} \qquad (53)$$

Additionally, bandwidth limits of the op amp are an issue. However, this can be mitigated by the two-pole input filter option. This allows the op amp to be "cocooned" within filtering that prevents signals beyond its specified bandwidth from reaching it. This would seem to be a more logical strategy than the typical GBW > 10X loop bandwidth that's often assumed with op-amp circuits. See the online version for further discussion.

Next, we consider the op-amp output current limits on C_4. We are used to seeing strict limits on op amps, but against a capacitor (not a pure dc load), many can drive loads of 10 Ω and sometimes even less. But, with a large frequency change on the PLL, that capacitance does take large current that may exceed the op-amp max in the range of 10 to 100 mA. Fundamentally, we desire the op-amp max current I_{opmax} to be able to charge C_4 at the same rate that $D_c{*}I_{pd}$ charges C_2 during a large frequency change. Using I*t = CV:

$$C_{4max} = \frac{I_{opmax} C_2}{D_c I_{pd}} \qquad (54)$$

This maximum is sometimes more than we would like to use due to size and cost reasons, possibly leading to resistor values too small for the op amp. In that case, we select a value of R_4 that allows for thermal noise considerably less than that of the op amp. We then find $C_4 = T_4/R_4$.

WHAT'S NEXT

The transfer-function approach presented here leads to noise sources and shaping in article 2 of the series, along with revealing the key innovations driving full integration and how discrete VCO makers can fight back. Article 3 will focus on key parts and CAD tools that are the weapons of the low-noise synthesizer designer. Article 4 will put it all together with requirements and examples of integrated and discrete VCO synthesizers to meet them. mw

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REFERENCES

1. *"Digital PLL Frequency Synthesizers: Theory and Design"*, Ulrich L. Rohde, Prentice-Hall, 1983.

2. *"PLL Performance, Simulation, and Design"*, Dean Banerjee, First Edition 1998. The 5th edition of 2017 of this outstanding reference may be freely downloaded at: http://www.ti.com/tool/pll_book.

3. *"Phaselock Techniques,"* 2nd Ed, Floyd Gardner, John Wiley and Sons, 1979.

4. *"Phase Locked Loops,"* Third Edition, Roland Best, McGraw-Hill, 1997.